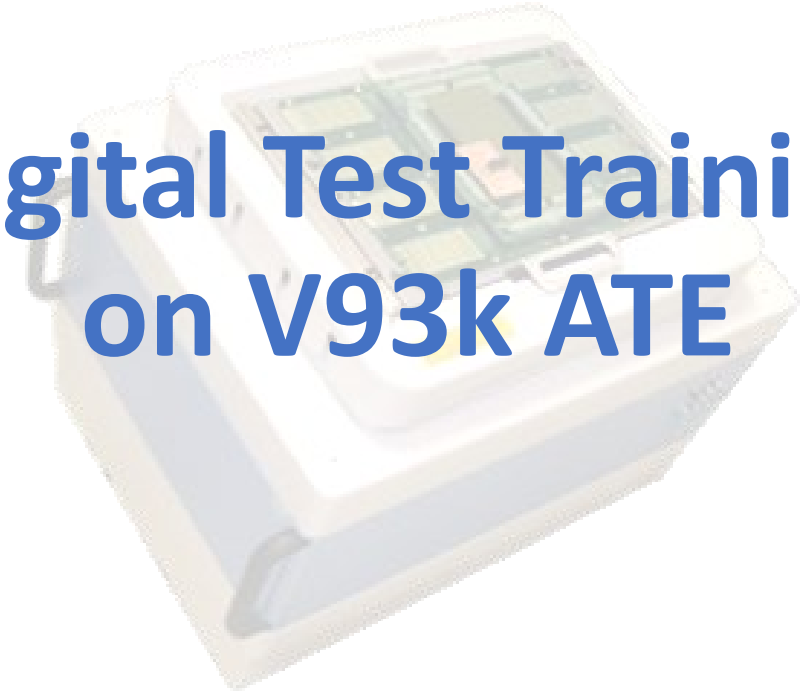
Industrial Test of Integrated Circuits



Digital Test Training on V93k ATE

M2 2024-25: ORGANIZATION

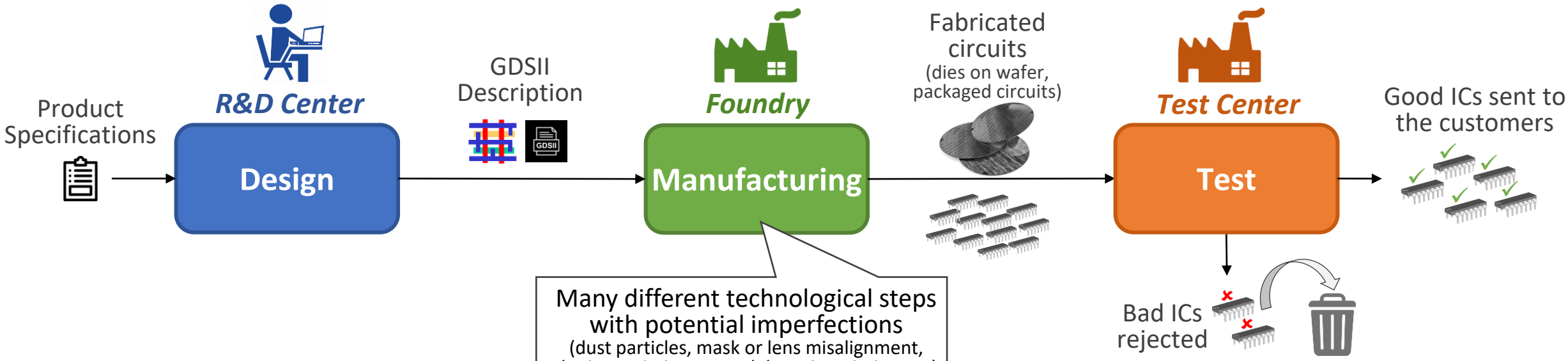
- Planning: 5 sessions

#	Date	Duration
1	September 9th 14h00-15h30	1.5hrs
2	September 9th 15h30-18h30	3hrs
3	September 23rd 14h00-17h00	3hrs
4	September 30th 14h00-17h00	3hrs
5	November 4th 14h00-17h00	3hrs
Total		***13.5hrs***

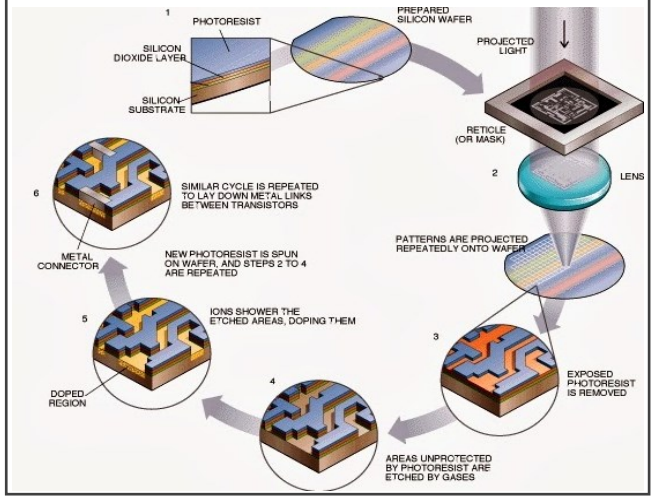
- "Integrated course"
  - Mix of lectures & labs/exercises during all sessions
- Evaluation
  - No formal exam but continuous assessment
  - Mini-tests performed during the sessions
  - Final grade: Sum of mini-test scores

CONTEXT

- Major steps in the production of Integrated Circuits



Many different technological steps with potential imperfections
(dust particles, mask or lens misalignment, doping variations, metal deposit variations, …)



Why Testing?

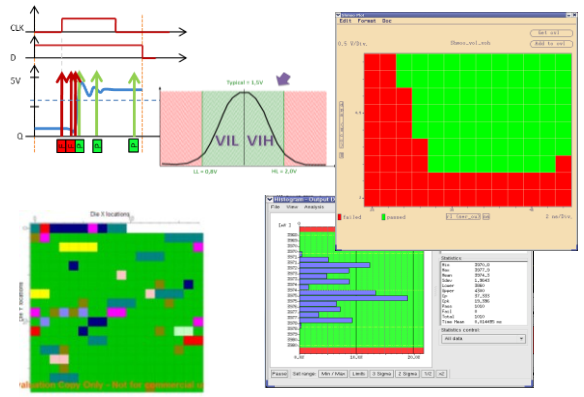
Test is an <u>essential step</u> as it guarantees the <u>quality</u> of the ICs delivered to the customers

OBJECTIVE OF THIS COURSE

- Acquire the fundamentals of digital ICs **industrial testing** ?

Pre-production
(first thousands of pieces)

Characterization tests
- Measurement values

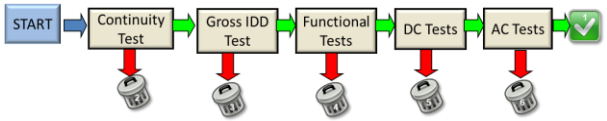


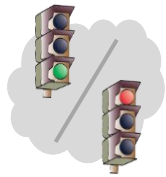
- Design & Manufacturing adjustments
- Basis for mass-production test program

ATE

Mass-volume production
(further millions of pieces)

Go/no-go tests
- Pass/Fail results





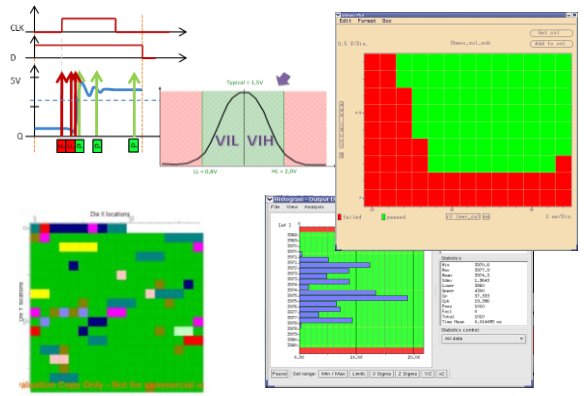
- Test time: major factor contributing to the testing costs
- Responsible for the quality of devices sent to customers

OBJECTIVE OF THIS COURSE

- Acquire the fundamentals of digital ICs industrial testing

Pre-production
(first thousands of pieces)

Characterization tests
- Measurement values



- Design & Manufacturing adjustments
- Basis for mass-production test program

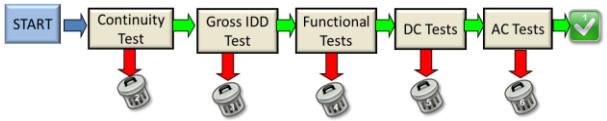
ATE

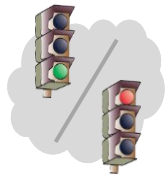
Concepts

- Equipment
  - HW: Physical resources of the ATE
  - SW: Tools to control the ATE
- Test Program
  - Test methods
  - Test flow
  - Test results analysis
  - Debug & diagnosis

Mass-volume production
(further millions of pieces)

Go/no-go tests
- Pass/Fail results





- Test time: major factor contributing to the testing costs
- Responsible for the quality of devices sent to customers

INDUSTRIAL ENVIRONMENT

- Automatic Test Equipment (ATE)

TERADYNE LTXCredence ADVANTEST VERIGY

Test Floor

TARGETED COMPETENCIES

Key Learnings

Concepts

- Equipment
  - HW: Physical resources of the ATE
  - SW: Tools to control the ATE
- Test Program
  - Test methods
  - Test flow
  - Test results analysis
  - Debug & diagnosis

Practical Implementation

Digital IC

74ACT299:
8-bit shift/storage register

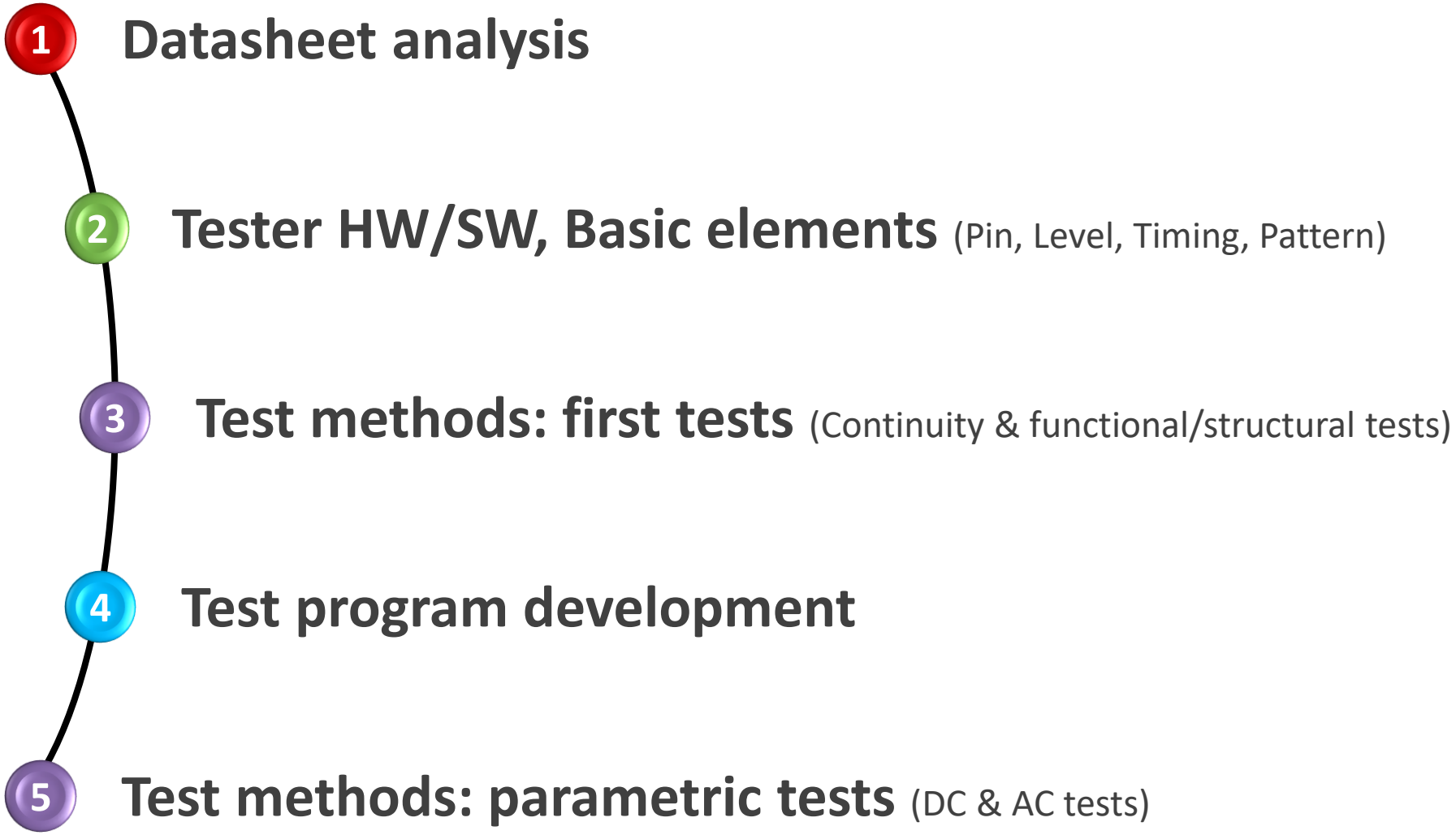
CNFM tester:
V93K

PASS

Functionality &
Performances

FAIL

LEARNING STEPS



PART 1

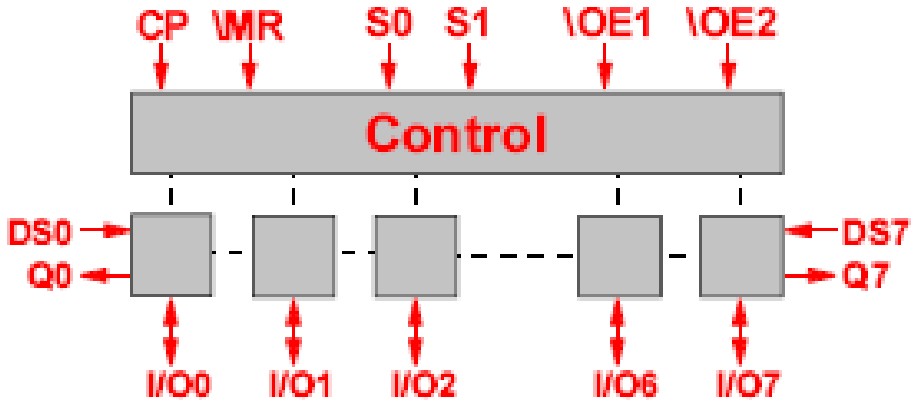
DATASHEET ANALYSIS

- **Device pins**
- **Functionality**
- **Operating conditions**
- **Performances** (typical/guaranteed limits)

1 DATASHEET ANALYSIS

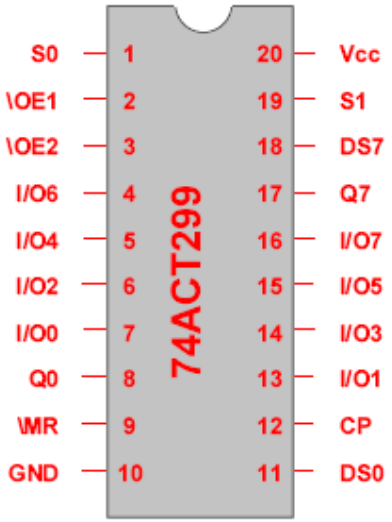
DEVICE UNDER TEST: 74ACT299

8- I/O universal shift/storage register



Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE_1}$, $\overline{OE_2}$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Pin Assignment



Basis to define pin configuration

1 DATASHEET ANALYSIS

FUNCTIONALITY: TRUTH TABLE

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐‾	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐‾	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐‾	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾ = LOW-to-HIGH Transition

- 4 Modes of operations controlled by (S_1, S_0)
  - Parallel Load: $(S_1, S_0) = 11$
  - Shift Right: $(S_1, S_0) = 01$
  - Shift Left: $(S_1, S_0) = 10$
  - Hold: $(S_1, S_0) = 00$
- Asynchronous reset controlled by $\overline{MR}$
  - active on $\overline{MR} = 0$

↳ Basis to develop functional test pattern

1 DATASHEET ANALYSIS

FROM DATA SHEET TO FUNCTIONAL TEST PATTERN

- Principle: Use of the truth table to define a test pattern (sequence of test vectors)
- Objective: Define a test pattern that checks all functionalities

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

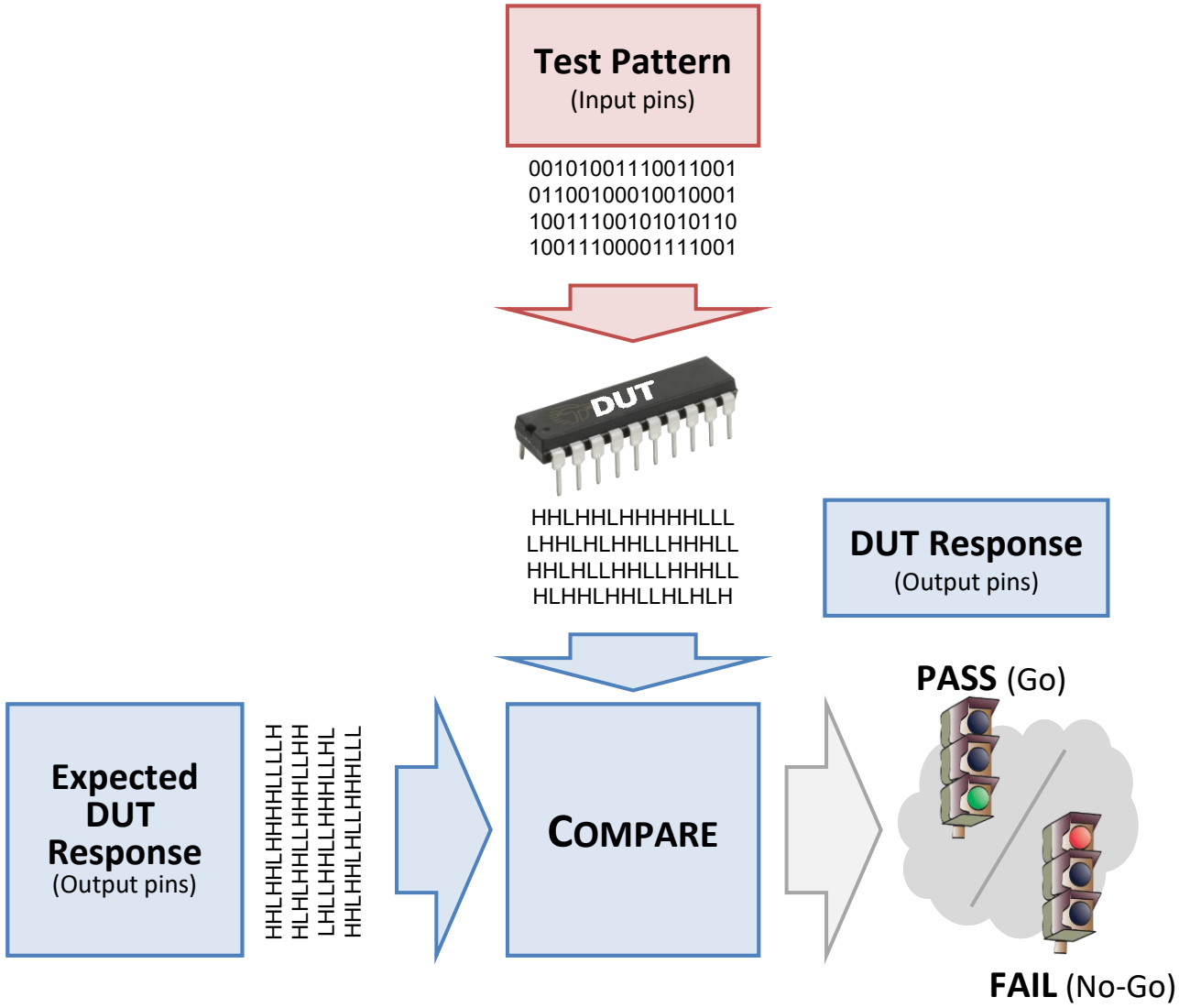
Master reset
Hold
Parallel Load (10000000)
Hold
Shift Right x8 – DS0=0
Parallel Load (01010101)
Shift Left x8 – DS7=1
…

MR	CP	S0	S1	DS0	DS7	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	Q0	Q7	INSTRUCTIONS
0	1	1	0	0	1	1	1	1	1	1	1	1	1	X	X	Master Reset
1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L	Hold
1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L	Parallel load
1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H	Shift right
1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L	Shift right
1	1	1	1	0	0	0	1	0	1	0	1	0	1	L	H	Parallel load
1	1	0	1	0	1	H	L	H	L	H	L	H	H	H	H	Shift left

1 DATASHEET ANALYSIS

FUNCTIONAL TEST CONCEPT

Test Result:
No Measurement Value
Only Pass/Fail



1 DATASHEET ANALYSIS

OPERATING CONDITIONS

DATA SHEET

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

TEST CONDITIONS FOR FUNCTIONAL TESTS

- Supply Voltage (V_{cc})
  - V_{cc} min $= 4.5V$ *
  - V_{cc} nom $= 4.75V$ *
  - V_{cc} max $= 5.0V$ *
- Operating Temperature
  - Cold: $-40°C$
  - Room: $+25°C$ *
  - Hot: $+85°C$ *

*** Production Test**

1 DATASHEET ANALYSIS

PERFORMANCES

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = 25°C$ Typ	74ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACT $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±5.5	±3.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

CLASSICAL PARAMETRIC DC TESTS

- Voltage
  - Input pins: V_{IH}/V_{IL}
  - Output pins: V_{OH}/V_{OL}
- Current
  - Input pins: I_{IN} *(leakage)*
  - Supply: I_{CC} *(consumption)*

↳ Limit values for parametric DC tests

(& test conditions)

1 DATASHEET ANALYSIS

PERFORMANCES

AC Electrical Characteristics for ACT *(Outputs)*

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t_{PLH}	Propagation Delay CP to I/O_n	5.0	4.5	8.5	12.5	4.5	13.5	ns
t_{PHL}	Propagation Delay CP to I/O_n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	4.0	14.0	15.0	4.0	18.0	ns
t_{PHL}	Propagation De $\overline{MR}$ to I/O_n							
t_{PZH}	Output Enable $\overline{OE}$ to I/O_n							
t_{PZL}	Output Enable $\overline{OE}$ to I/O_n							
t_{PHZ}	Output Disable $\overline{OE}$ to I/O_n							
t_{PLZ}	Output Disable $\overline{OE}$ to I/O_n							

Note 9: Voltage Range 5.0 is 5.

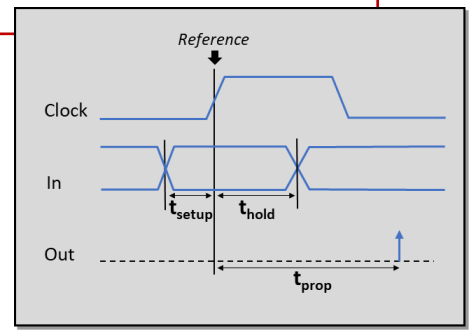
AC Operating Requirements for ACT *(Inputs)*

Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.5	ns
t_H	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	−2.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.0	ns
t_H	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	−1.0	1.0	1.0	ns
t_W	CP Pulse Width HIGH or LOW					
t_W	$\overline{MR}$ Pulse Width, LOW					
t_{REC}	Recovery Time, $\overline{MR}$ to					

Note 10: Voltage Range 5.0 is 5.0V ± 0.5

CLASSICAL PARAMETRIC AC TESTS

- Input pins
  - Setup Time
  - Hold Time
- Output pins
  - Propagation delay

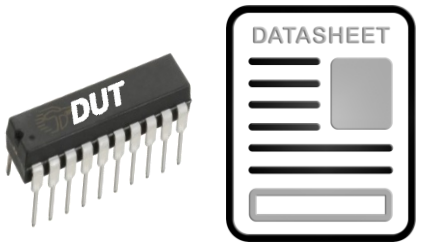


Limit values for parametric AC tests

(test conditions)

1 DATASHEET ANALYSIS

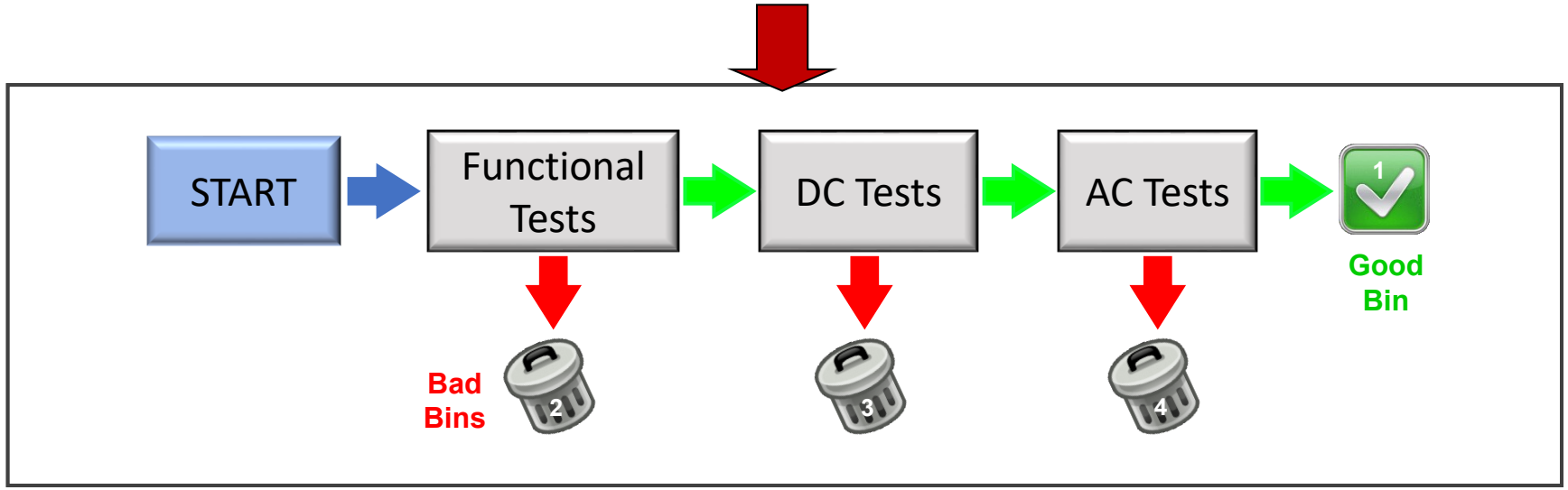
SUMMARY: FROM DATASHEET TO TEST PLAN



TEST PLAN

- **Functional tests**: @V_{cc}nom, @V_{cc}min & @V_{cc}max → ❶ **Functionality**
- **DC tests**: V_{IL}/V_{IH}, V_{OL}/V_{OH}, leakage current, I_{cc}
- **AC tests**: setup time, hold time, propagation delay

❷ **Performances**



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Exercises:
74ACT299 Datasheet Analysis

PART 2

- HW resources
- SW interface
- Basic elements
  - Pin
  - Level
  - Timing
  - Pattern

2 TESTER HW/SW

OVERVIEW

Cooling Unit

Main Frame

Fiber-optic Transmission

DUT Board

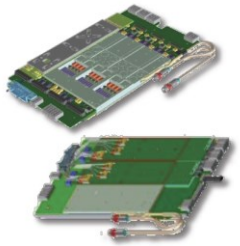
Manipulator

Test Head

Workstation
(LINUX PC)

SmarTest® SW
- Offline mode
- Online mode

Pin Electronics



- Supply
- Digital
- Analog
- RF

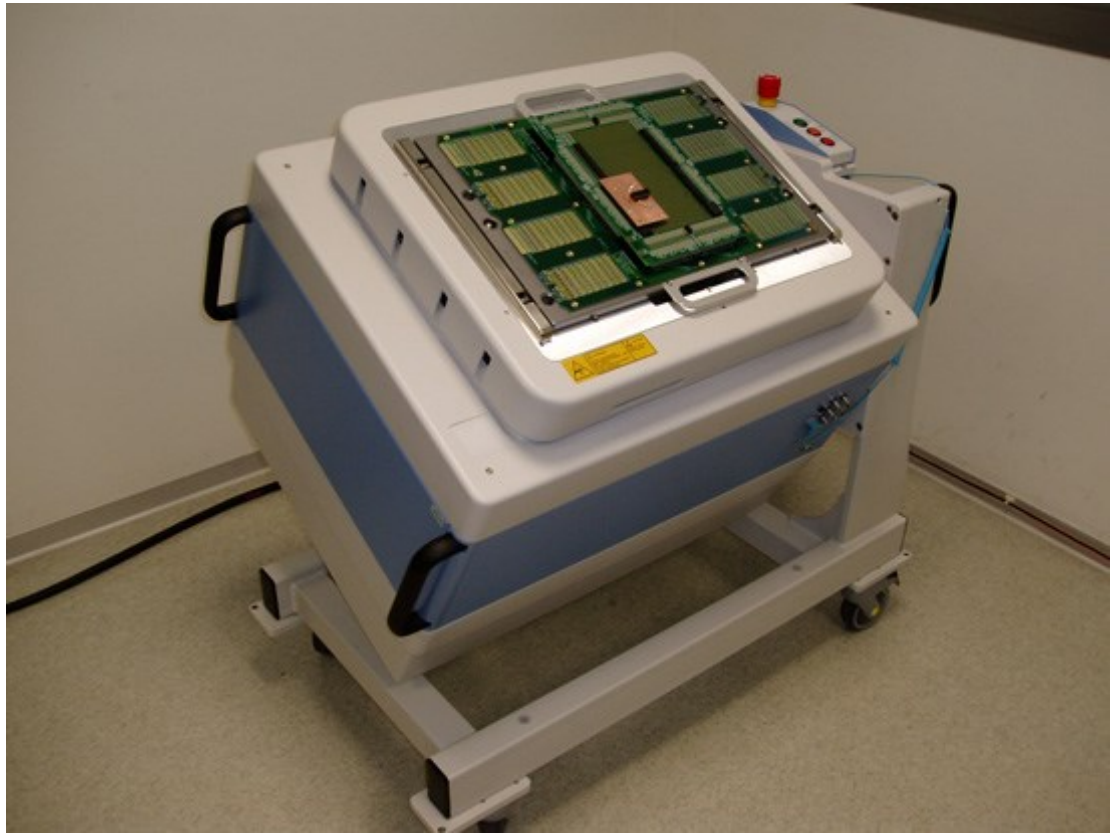
CNFM TESTER: COMPACT VERIGY V93K PINSCALE

64 **Digital pins**
=> 200 Ks/s up to 3.6 Gs/s

8 **Device Power Supply pins**

4 **Analog Source pins**
=> Audio: 1.024 Msps, 24-bit
=> Video:100 Msps, 14-bit

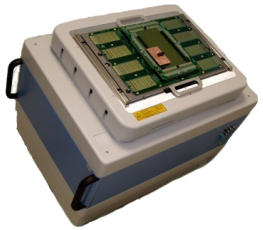
4 **Analog Digitizer pins**
=> Audio: 200ksps, 24-bit, 50kHz BW
=> Video : 65Msps, 14-bit, 15MHz BW/100MHz



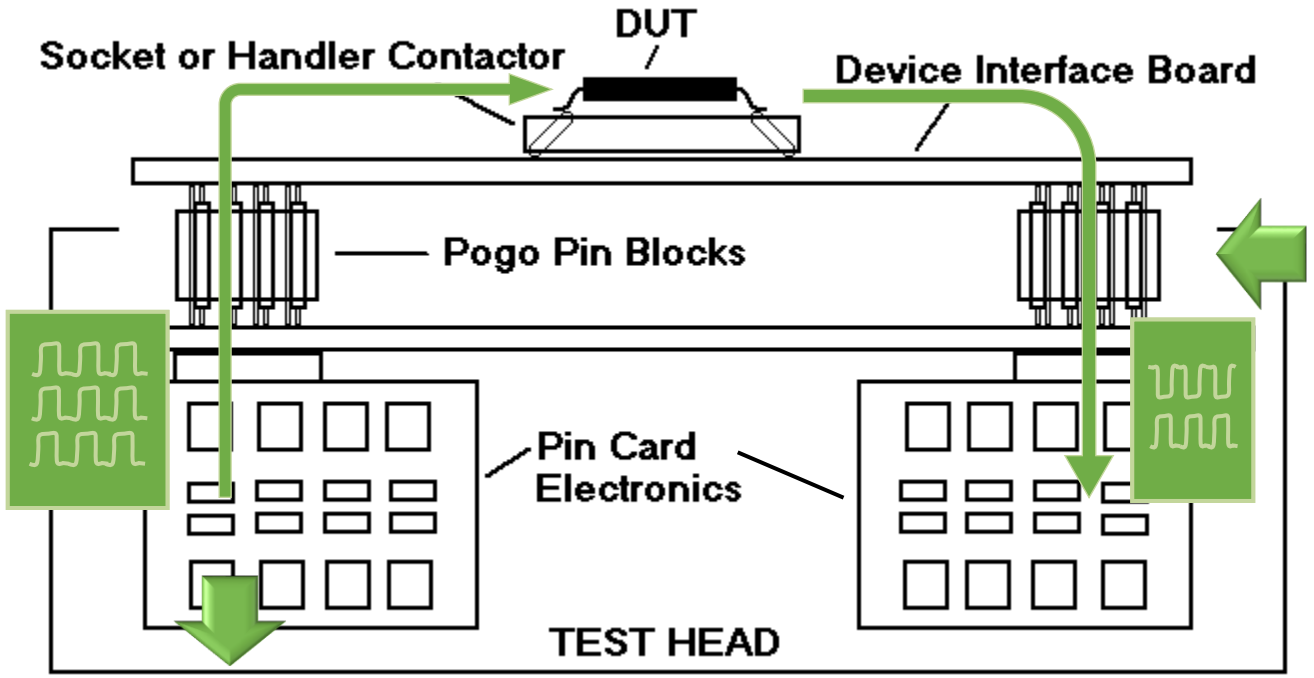
2

Introduction to Tester Hardware

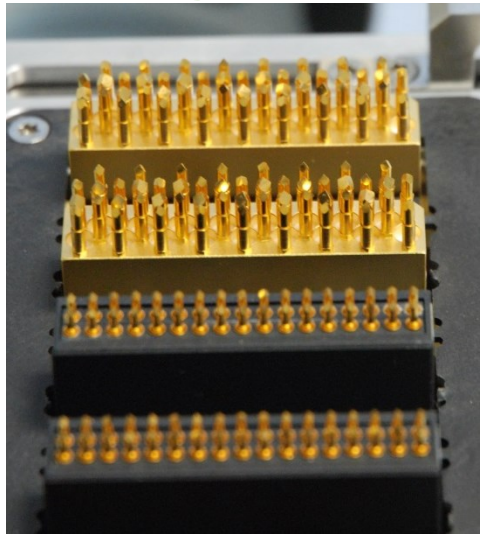
2 TESTER HW



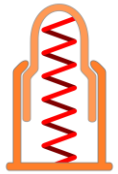
FROM TESTER TO DUT

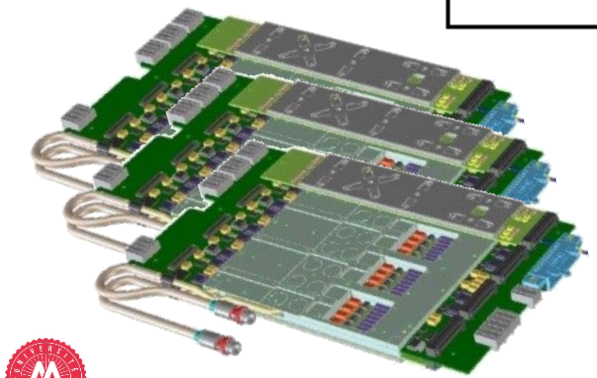


Pogo Pins



Pogo Pin:
Specific electrical connector with an integrated helical string (high durability and good resilience to mechanical shock and vibration)

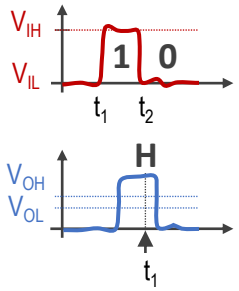


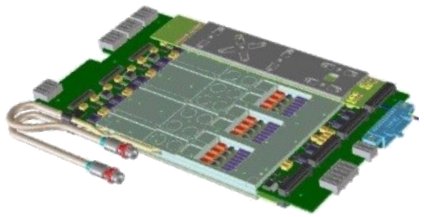


- Device Power Supply
- Clock board
- Pin Electronics (PE)

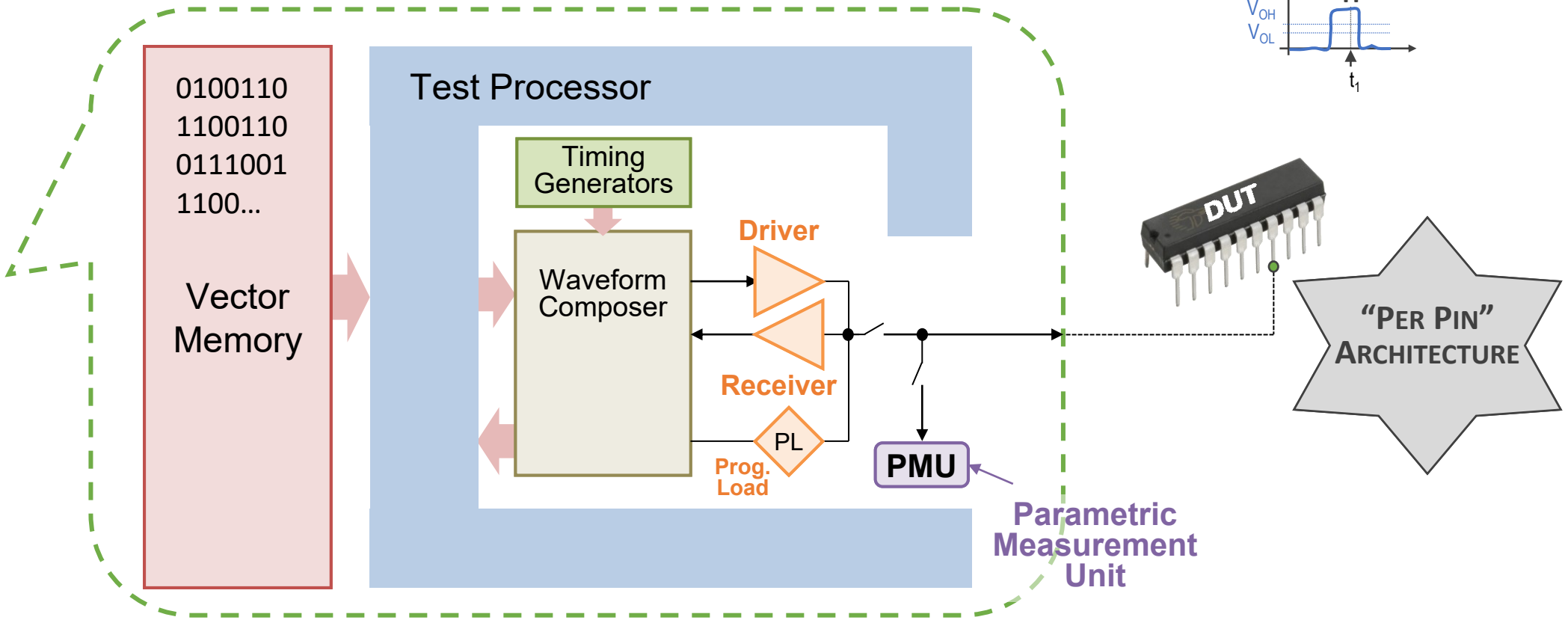
PIN ELECTRONICS

Electrical signal = Combination of level and timing information



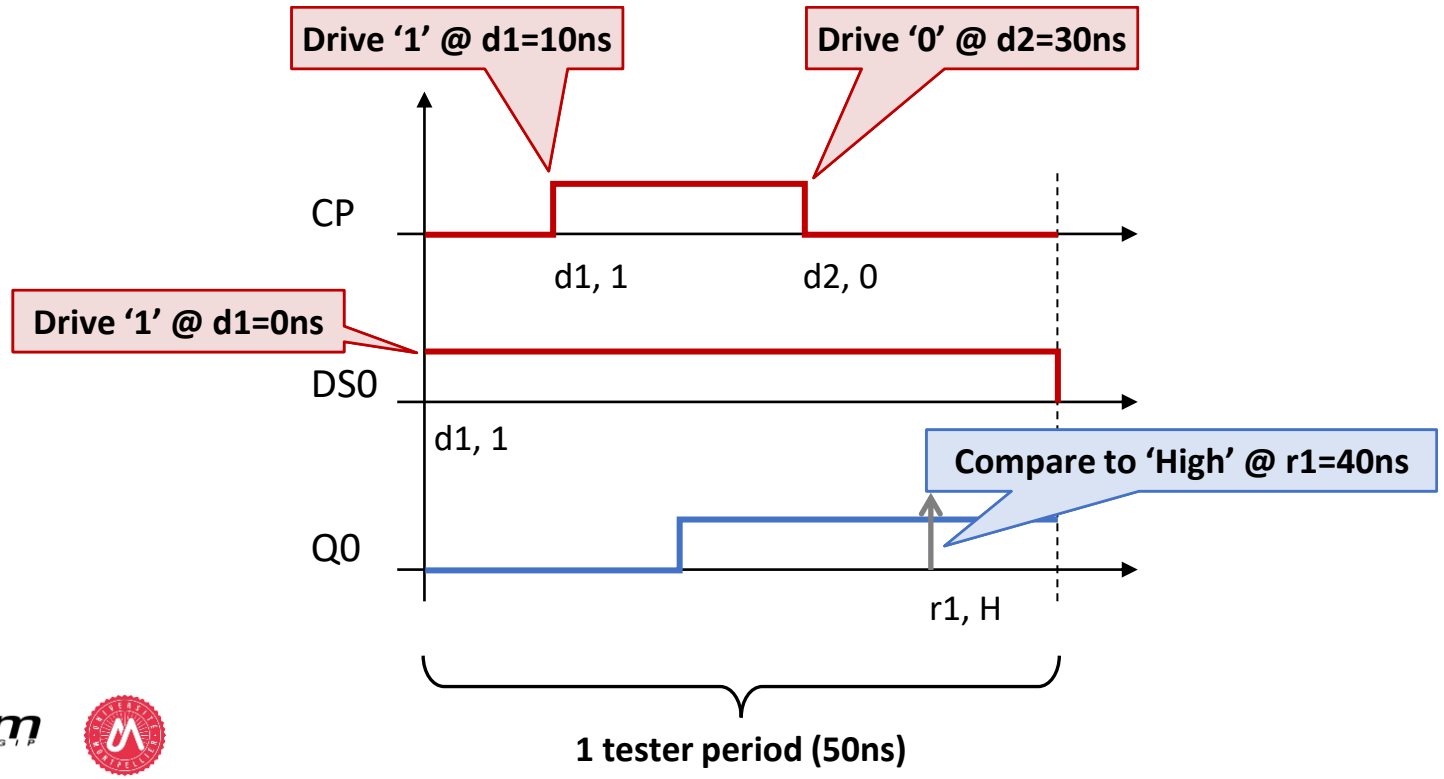


PE



PIN ELECTRONICS - TIMING

- Concept
  - "**actions**" associated to "**edges**"
- Example



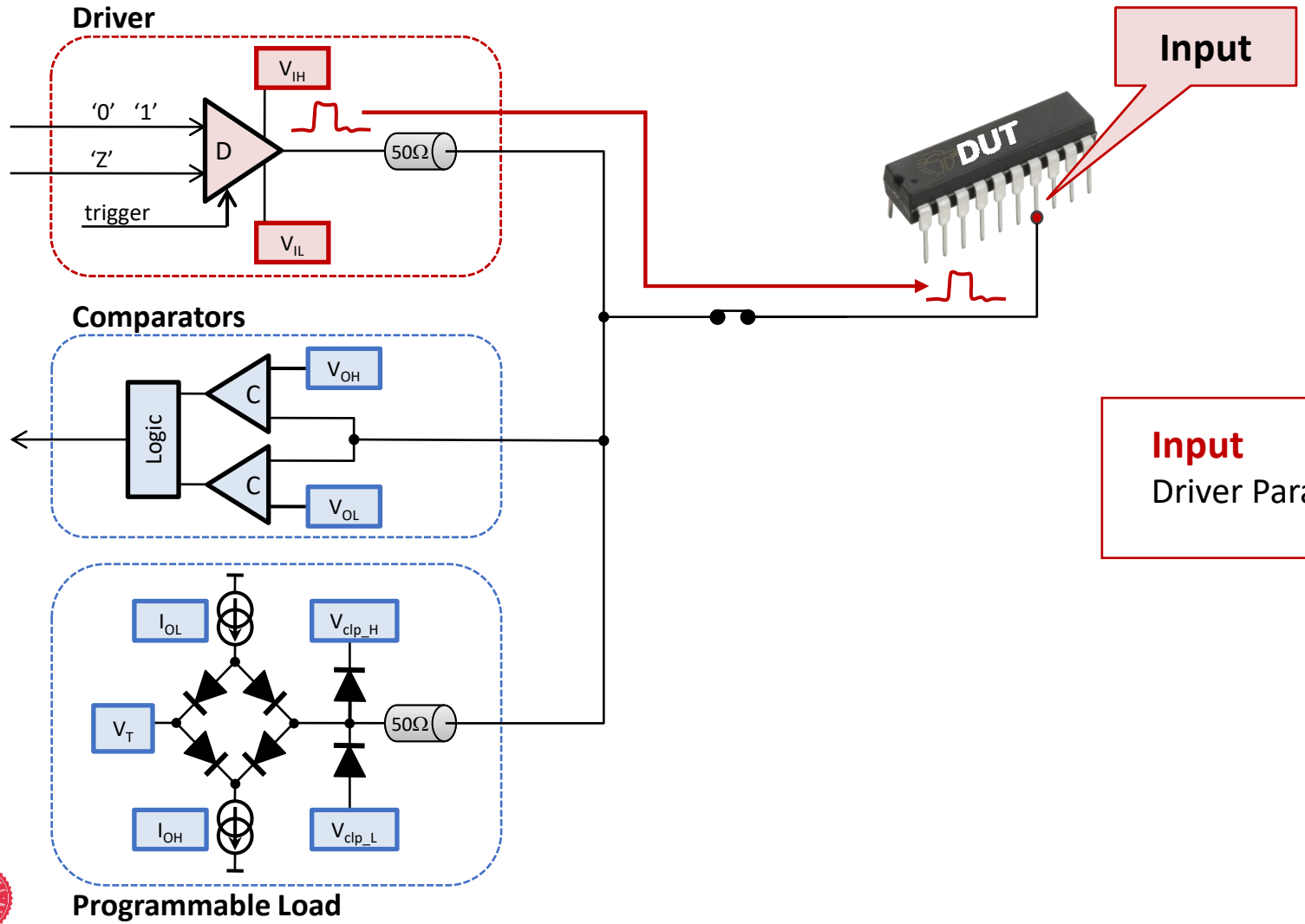
Tester timing resources per pin

- Input pins: 8 drive edges (d1, d2, …, d8)
- Output pins: 8 receive edges (r1, r2, …, r8)
- I/O pins: 8 drive edges + 8 receive edges

Actions

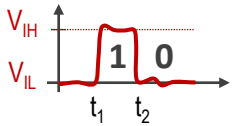
- Drive actions
  - 0: Drive '0'
  - 1: Drive '1'
  - Z: High impedance
  - N: No action
- Receive actions *(edges)*
  - L: Compare to 'Low'
  - H: Compare to 'High'
  - M: Compare to 'Intermediate'
  - X: Don't care

PIN ELECTRONICS - LEVEL

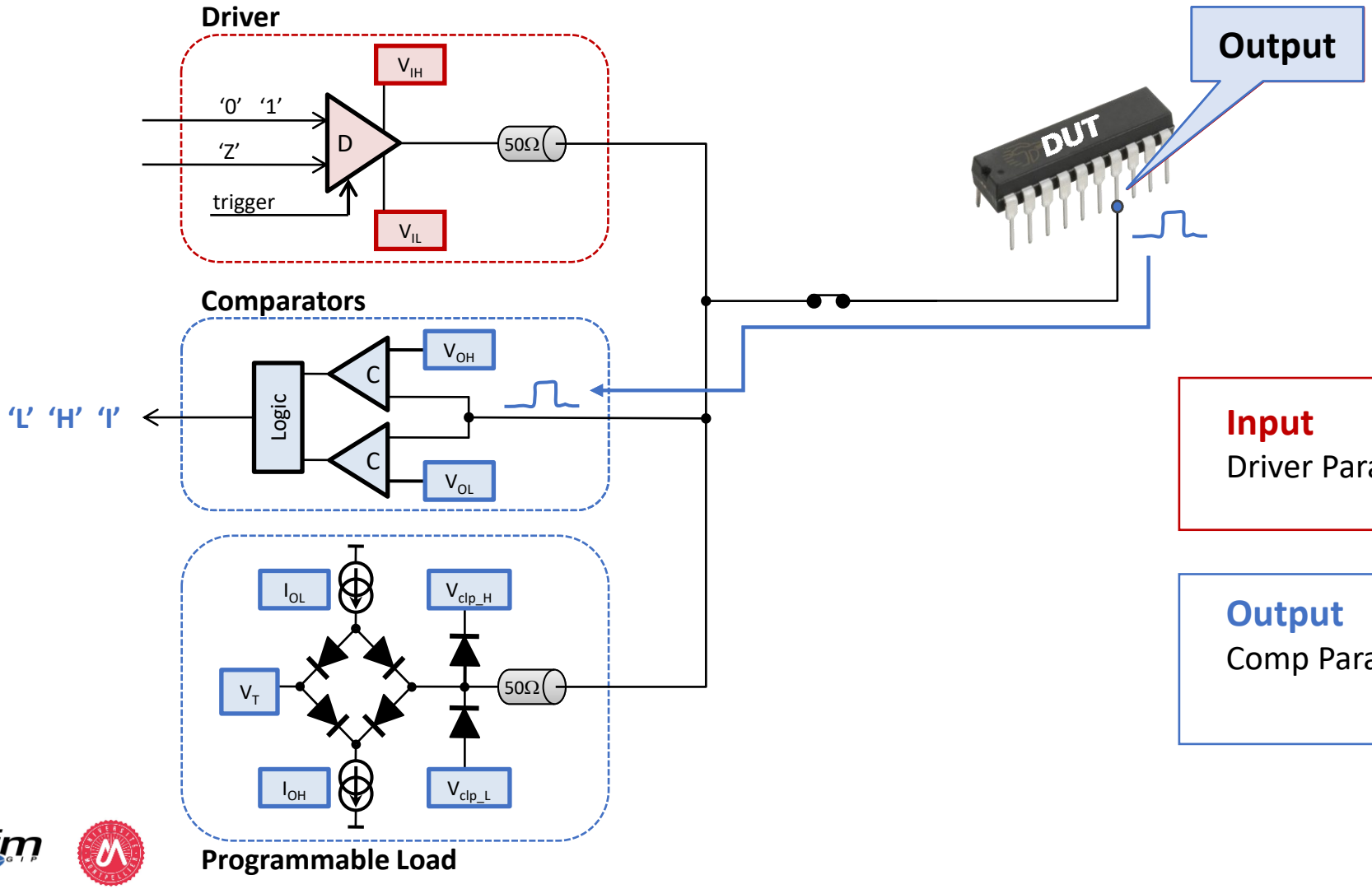


Input

Driver Parameters: V_{IL}, V_{IH}

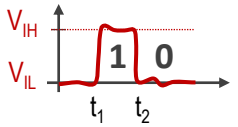


PIN ELECTRONICS - LEVEL



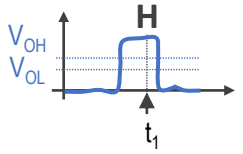
Input

Driver Parameters: V_{IL}, V_{IH}

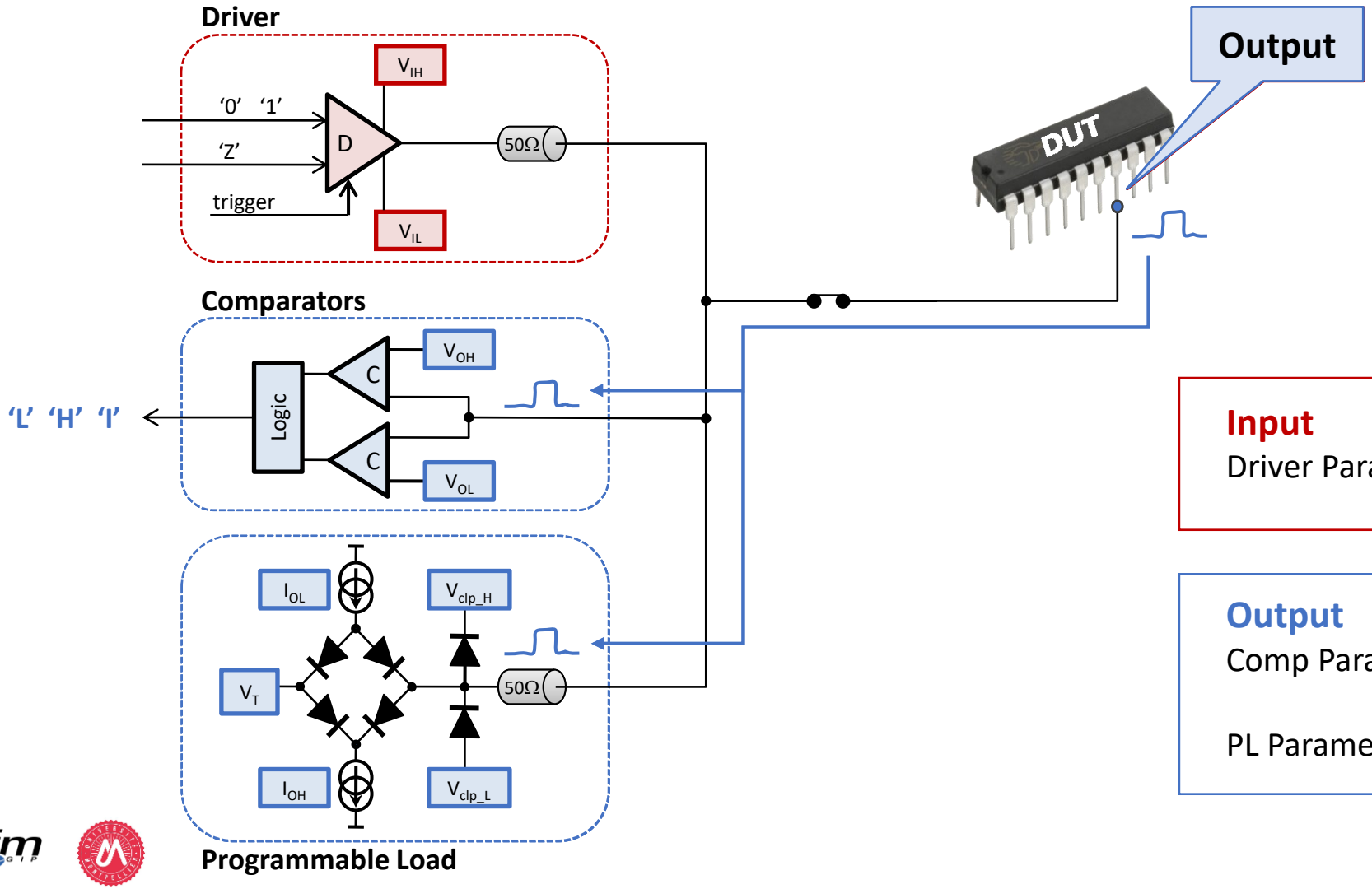


Output

Comp Parameters: V_{OL}, V_{OH}

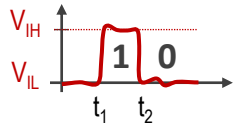


PIN ELECTRONICS - LEVEL



Input

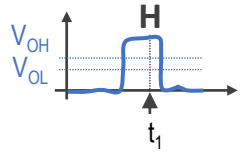
Driver Parameters: V_{IL}, V_{IH}



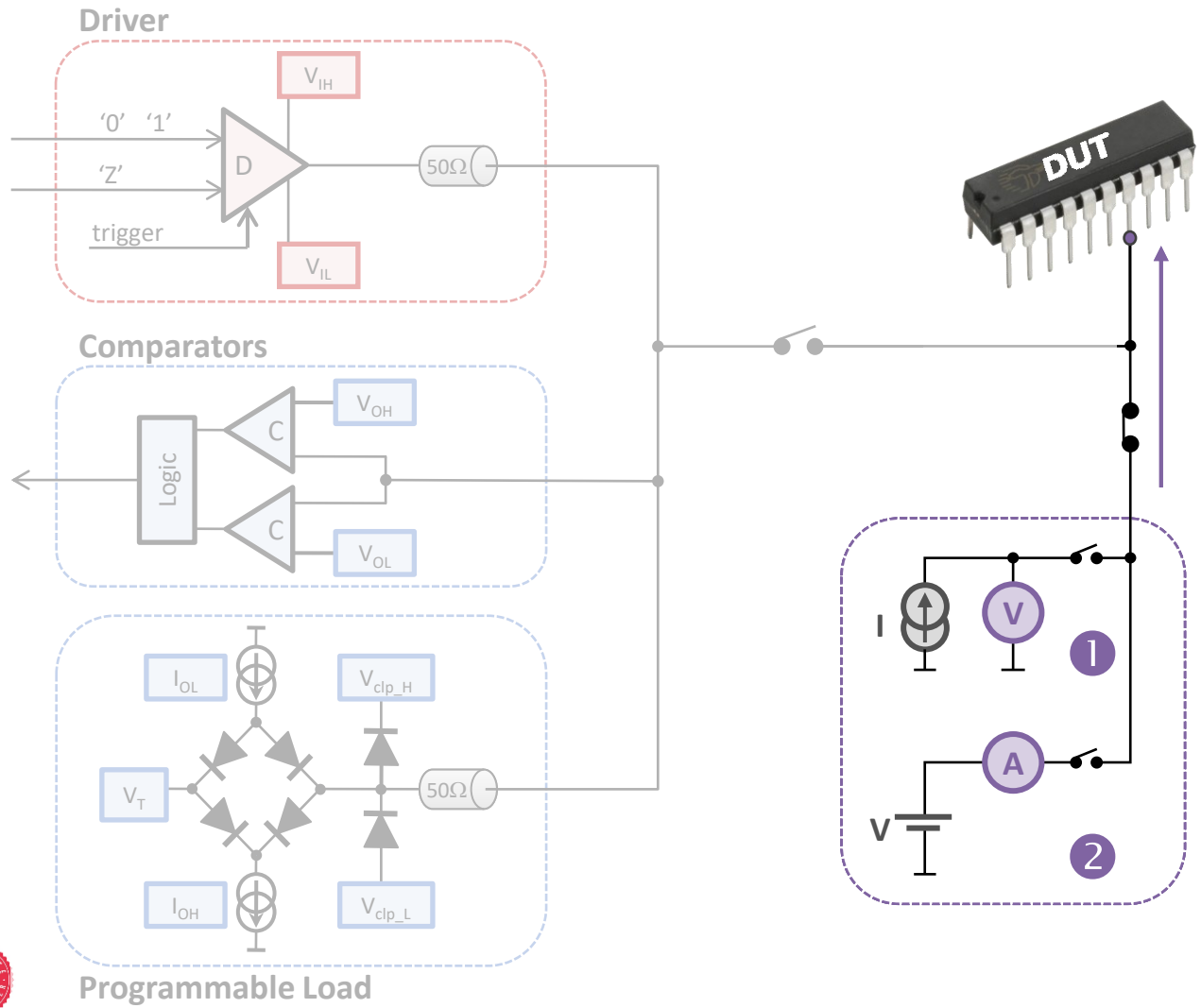
Output

Comp Parameters: V_{OL}, V_{OH}

PL Parameters: I_{OL}, I_{OH}, V_T, V_{clp_L}, V_{clp_H}



PIN ELECTRONICS - PMU

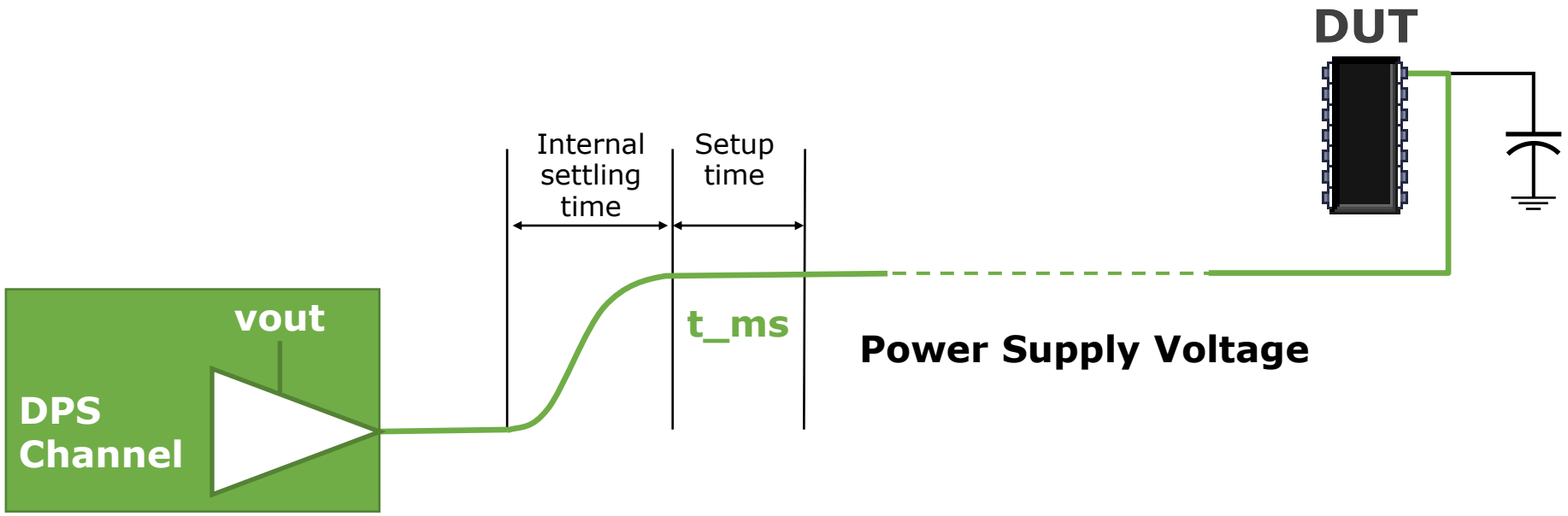


Parametric Measurement Unit

2 modes of operation

- Current generator & **Voltage Meas** 1
- Voltage generator & **Current Meas** 2

DEVICE POWER SUPPLY (DPS)



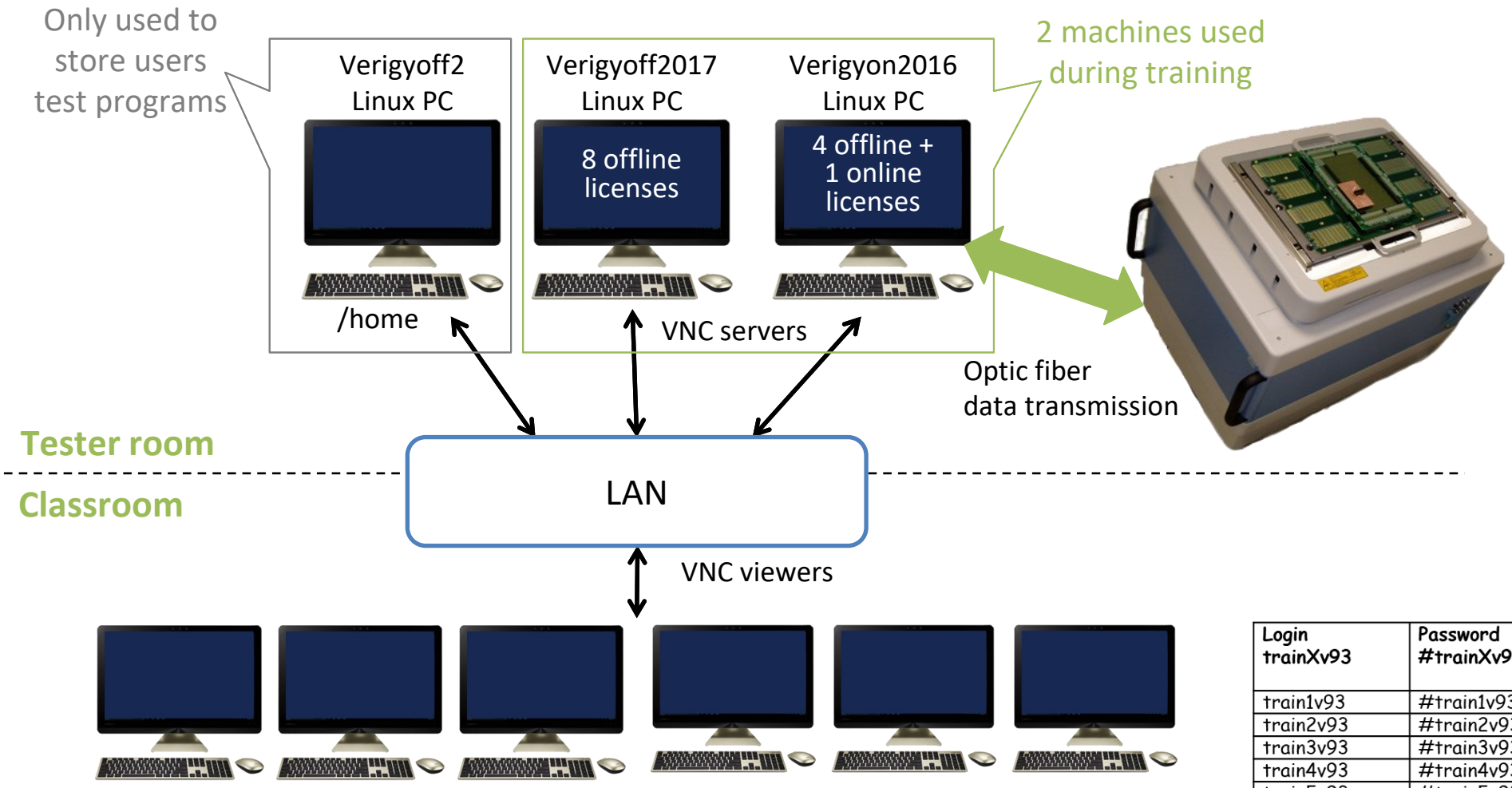
DPS parameters

- **vout** (V) power supply voltage
- **t_ms** (ns) setup time
- **ilimit** (A) connect current limit (to prevent destruction of the DUT)

2

Introduction to Tester Software "SmarTest"

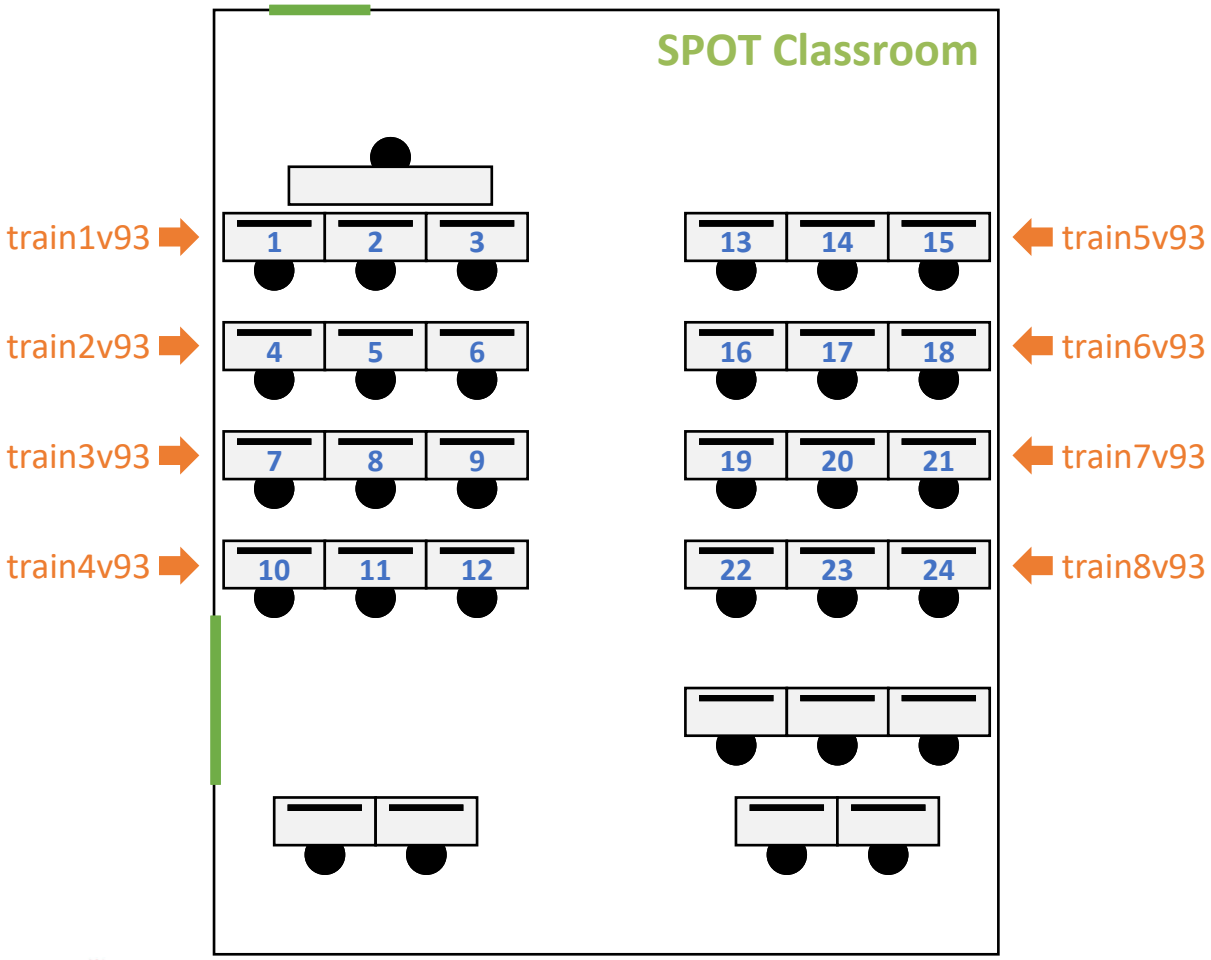
LAB ENVIRONMENT



24 desktops - 8 generic user accounts

Login trainXv93	Password #trainXv93#	Y: VNC display number
train1v93	#train1v93#	71
train2v93	#train2v93#	72
train3v93	#train3v93#	73
train4v93	#train4v93#	74
train5v93	#train5v93#	75
train6v93	#train6v93#	76
train7v93	#train7v93#	77
train8v93	#train8v93#	78

LAB ENVIRONMENT



Tester connection

Only 8 offline licenses run at the same time during practice (memory issues)

- 2 on verigyon2016
- 6 on verigyoff2017

Work in "trio"

Login trainXv93	Password #trainXv93#	Y: VNC display number	M: Default machine for offline connection
train1v93	#train1v93#	71	verigyon2016
train2v93	#train2v93#	72	verigyon2016
train3v93	#train3v93#	73	verigyoff2017
train4v93	#train4v93#	74	verigyoff2017
train5v93	#train5v93#	75	verigyoff2017
train6v93	#train6v93#	76	verigyoff2017
train7v93	#train7v93#	77	verigyoff2017
train8v93	#train8v93#	78	verigyoff2017

Local PC connection

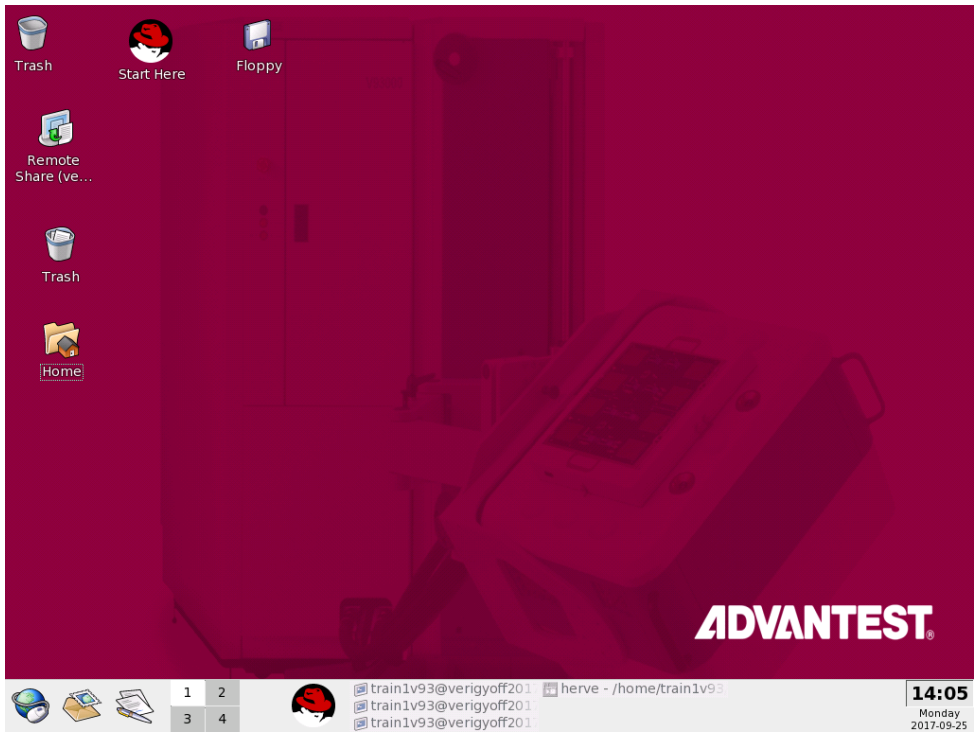
- Login: etudiant
- Password: &tudiant

LAB ENVIRONMENT

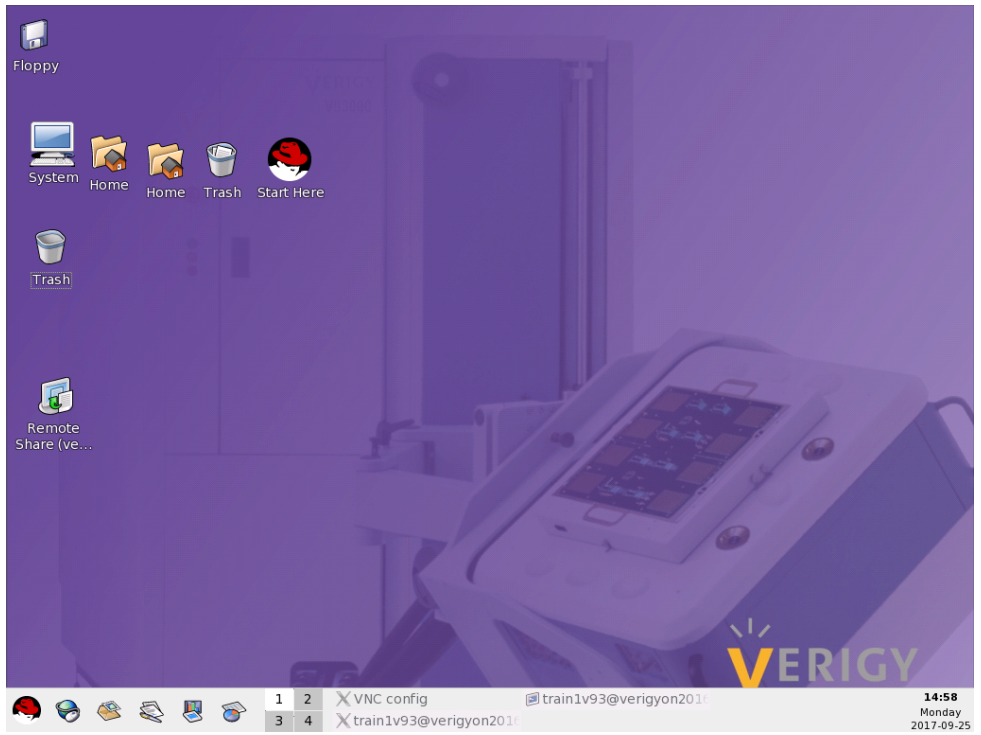
- Procedure to start Graphical Interface of tester SW

  1/ Connect to a **verigy** machine using **VNC**

Screen of verigyoff2017



Screen of verigyon2016

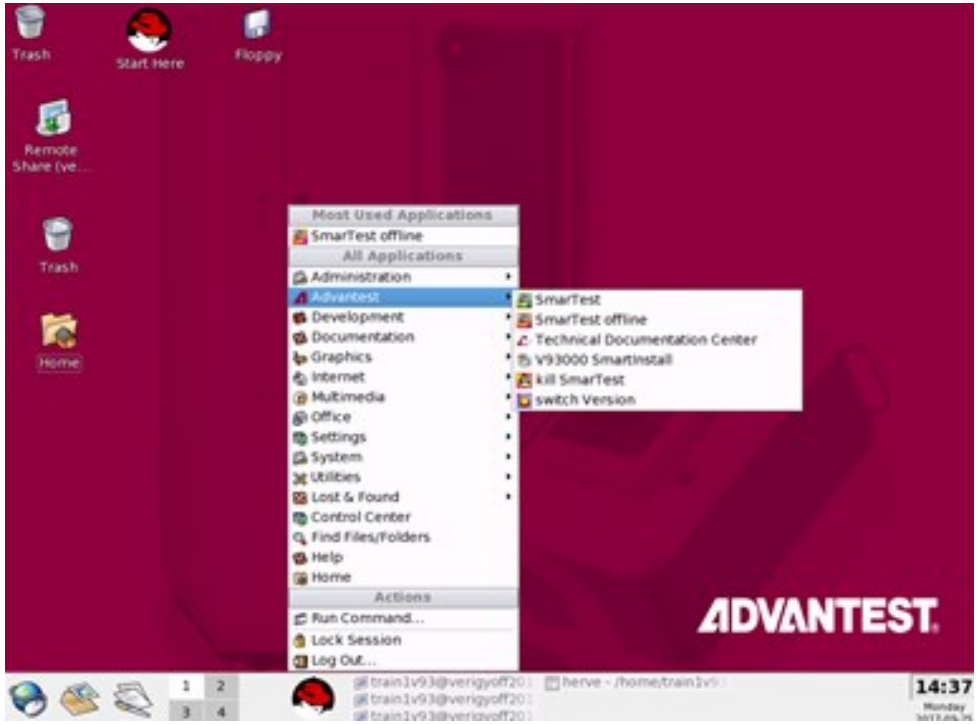


LAB ENVIRONMENT

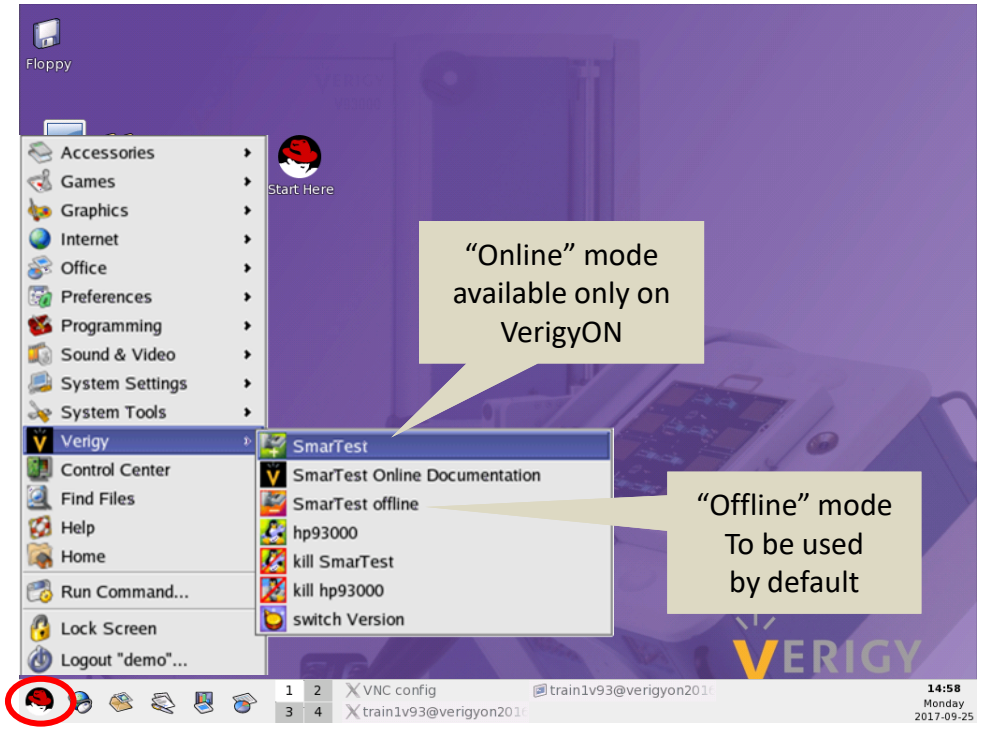
- Procedure to start Graphical Interface of tester SW

  2/ Launch **SmarTest** from the start menu “  ” (“RedHat” menu)

verigyoff2017

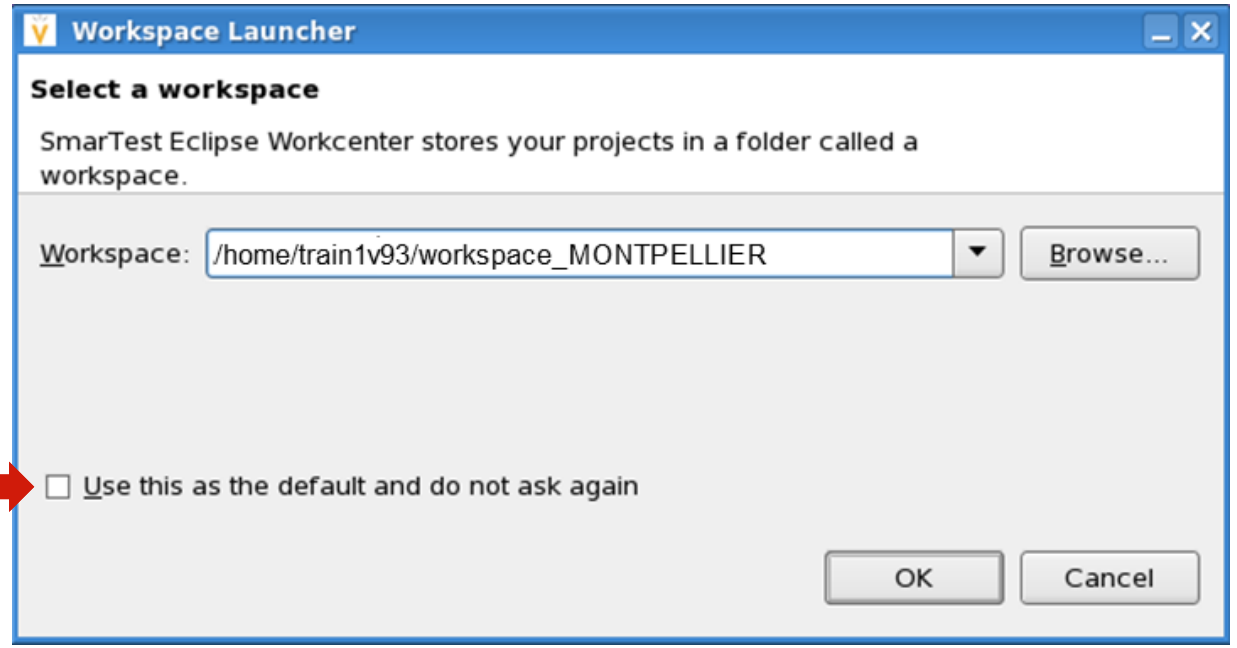


verigyon2016



AT STARTUP: WORKSPACE SELECTION

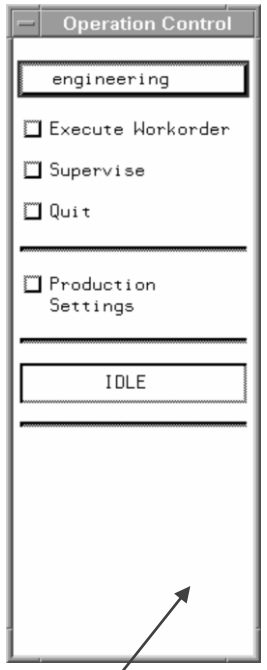
NEVER SELECT THIS OPTION



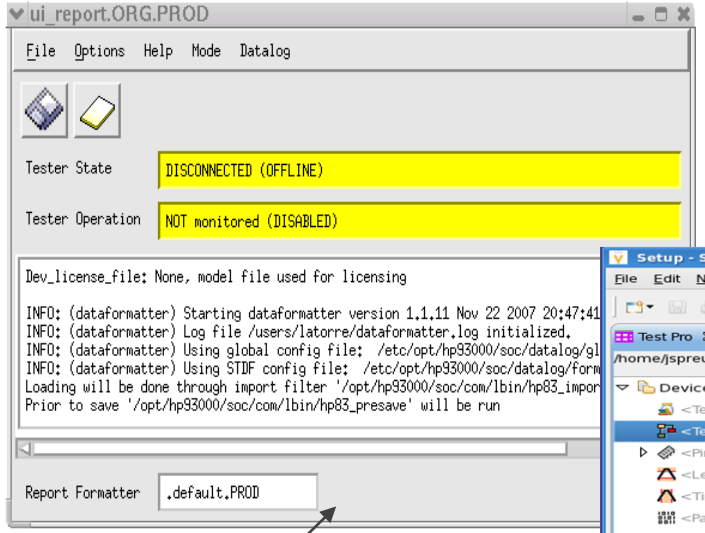
Workspace stores users' interface configuration

Do not mix it with test program explorer path

AT STARTUP: 3 WINDOWS

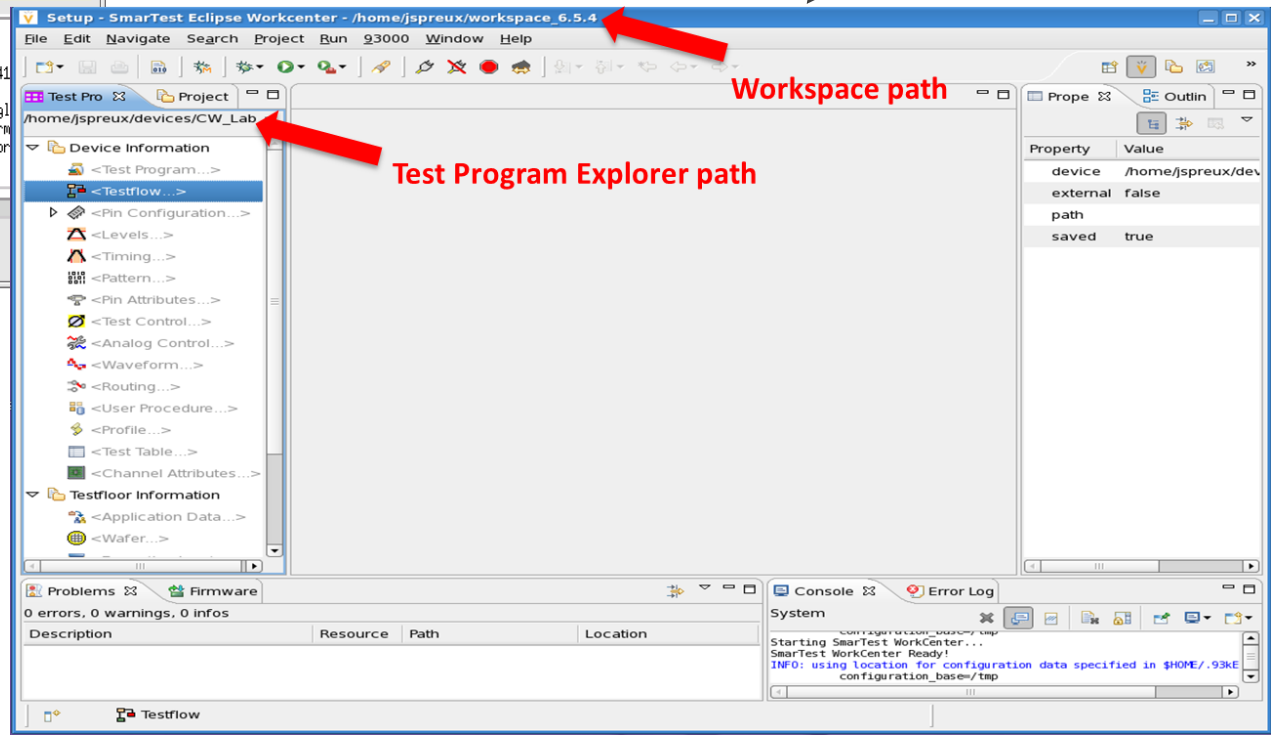


"Operation Control"
- Tasks execution
- Datalog Formatting

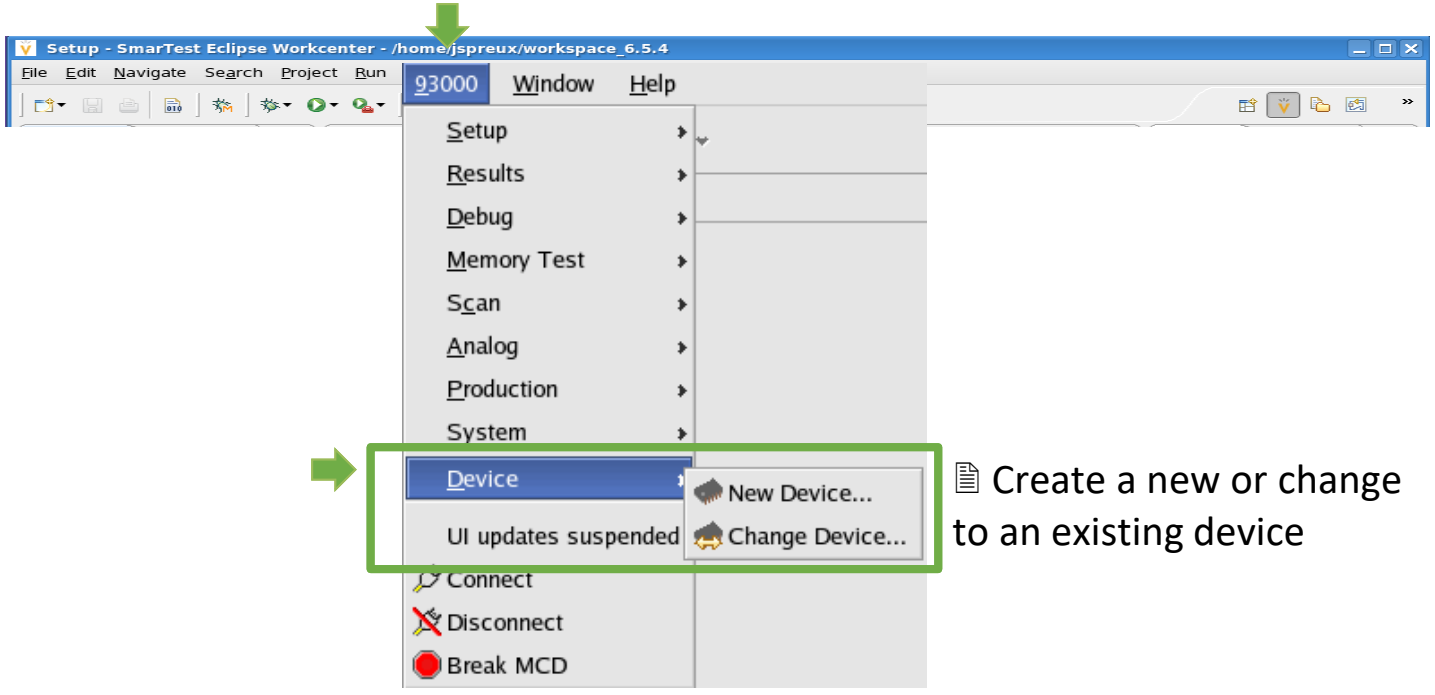


"ui_report"
- Syntax errors
- Test execution issues
- Test results

"SmarTest Eclipse Workcenter"
- **MAIN WINDOW**
- Provide all tools to:
  - Create & load configuration files
  - Create & execute a test flow
  - …



FIRST STEP: CREATE A DEVICE



Create a new or change to an existing device

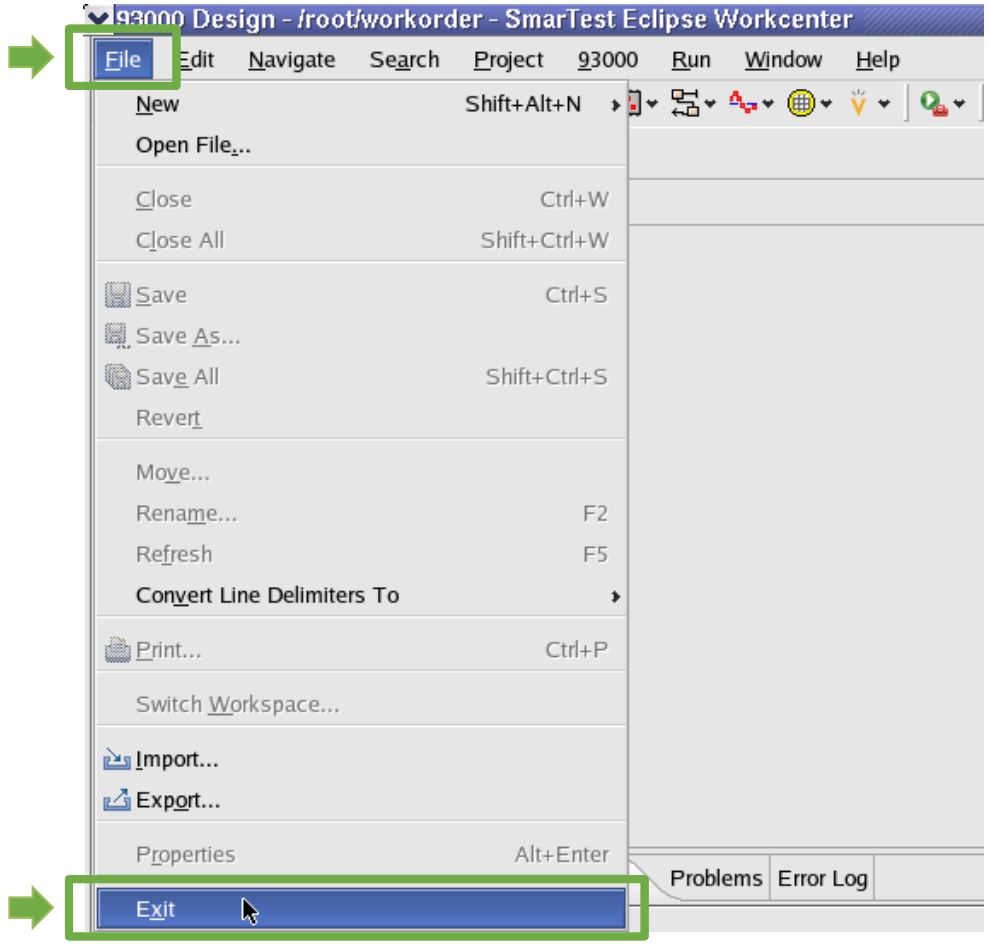
- To create a device, click

  93000 > Device > New Device

- Device creation will automatically generate all sub-directories necessary to develop & store the test program specific to this device

```
[root@localhost training]# ls -a
.               ch_attributes  license         scan          testprog
..              configuration  lock_file       scan_res      timing
.technology     data_set       memt_llapg      scrambling    timing_dgrm
analog_control  di_report      memt_patterns   shmoo         vectors
applicat        error_map      memt_repair     state_list    wafertyp
bitmap          fail_memory    pin_attributes  testflow      waste
bitmap_conf     format         report          testflow_vee  waveform
calibration     levels         routing         testfunc
```

EXITING SMARTEST

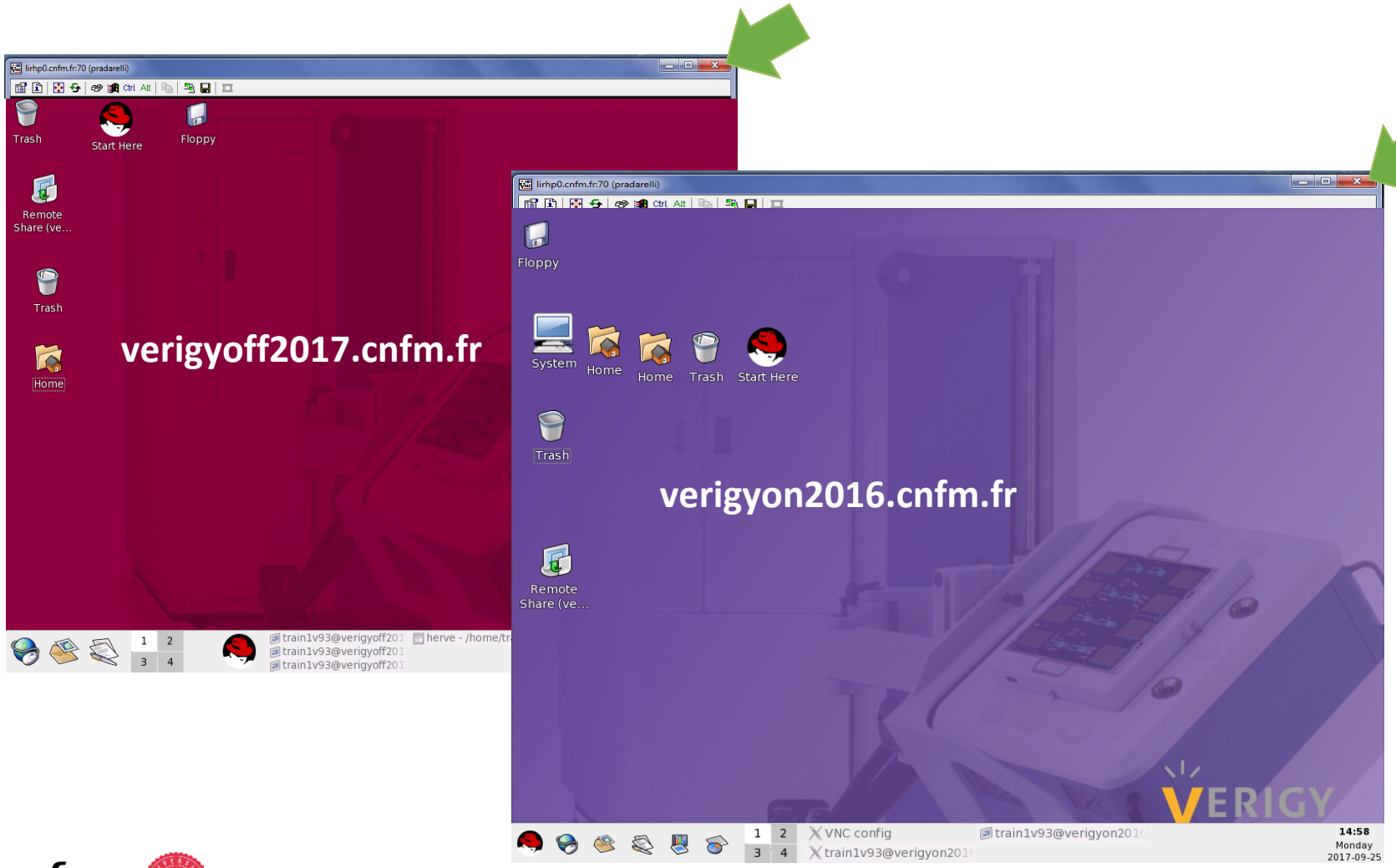


- To exit SmarTest, click **File > Exit**

To kill the entire SmarTest process, type the following command in a Terminal window:

/opt/hp93000/soc/prod_env/lbin/kill_smarTest

EXITING VNC



- Close the window to exit VNC

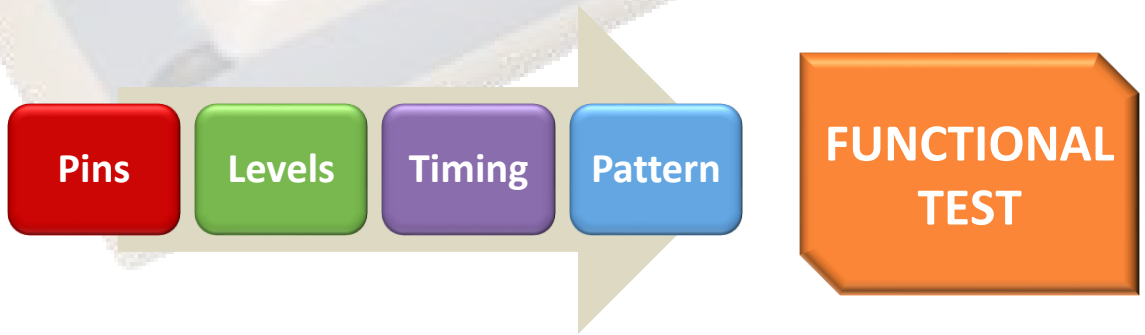
DO NOT LOGOUT!
=> VNC server must be launched again

2

Lab:
First Steps with SmarTest - Part 1

2

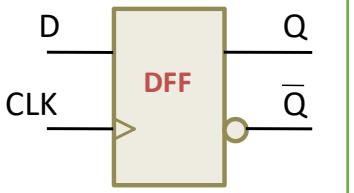
INTRODUCTION TO BASIC ELEMENTS

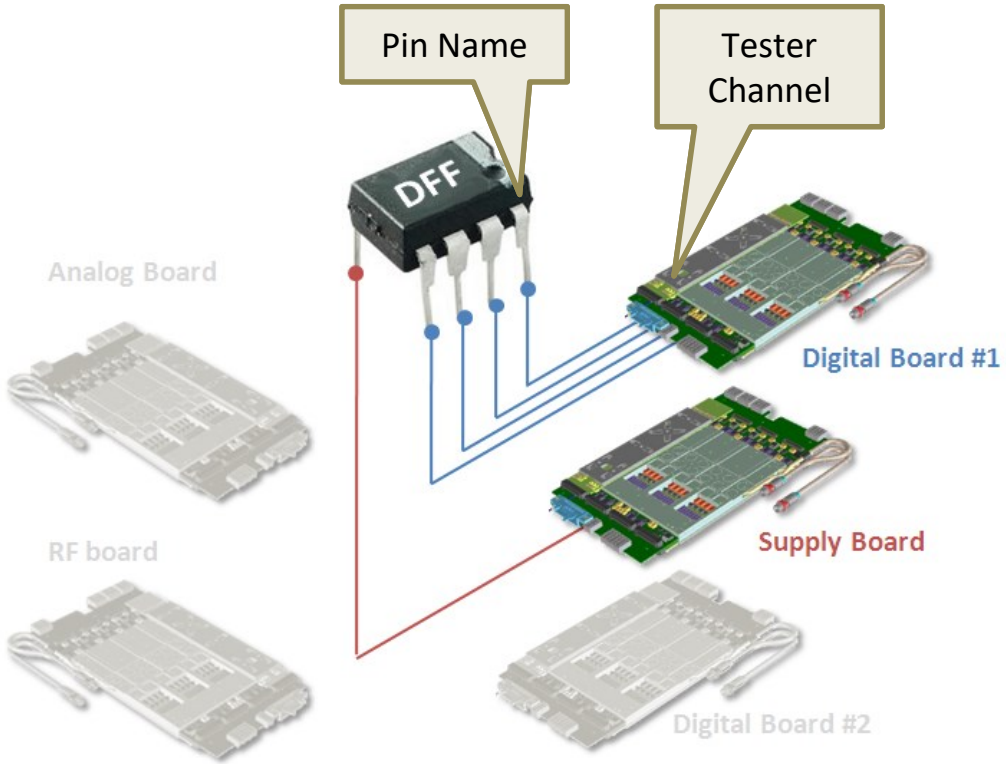


PINS

- First element to be defined
  - Link between **Pin Names** and **Tester Channels**
  - Definition of **Pin Type**

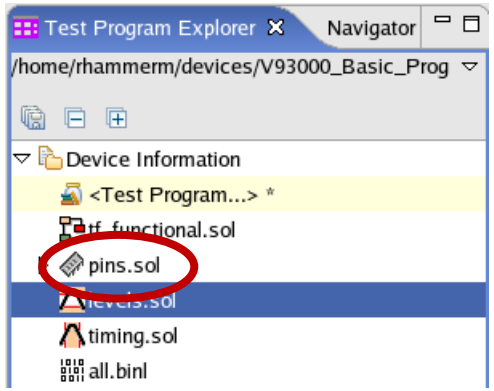
EXAMPLE





Pin Name	Pin Type	Tester Channel
CLK	Input	10101
D	Input	10102
Q	Output	10103
_Q	Output	10104
V_{CC}	Supply	10201

PIN SETTING IN SMARTEST



From Datasheet

From DIB

Pin Setting

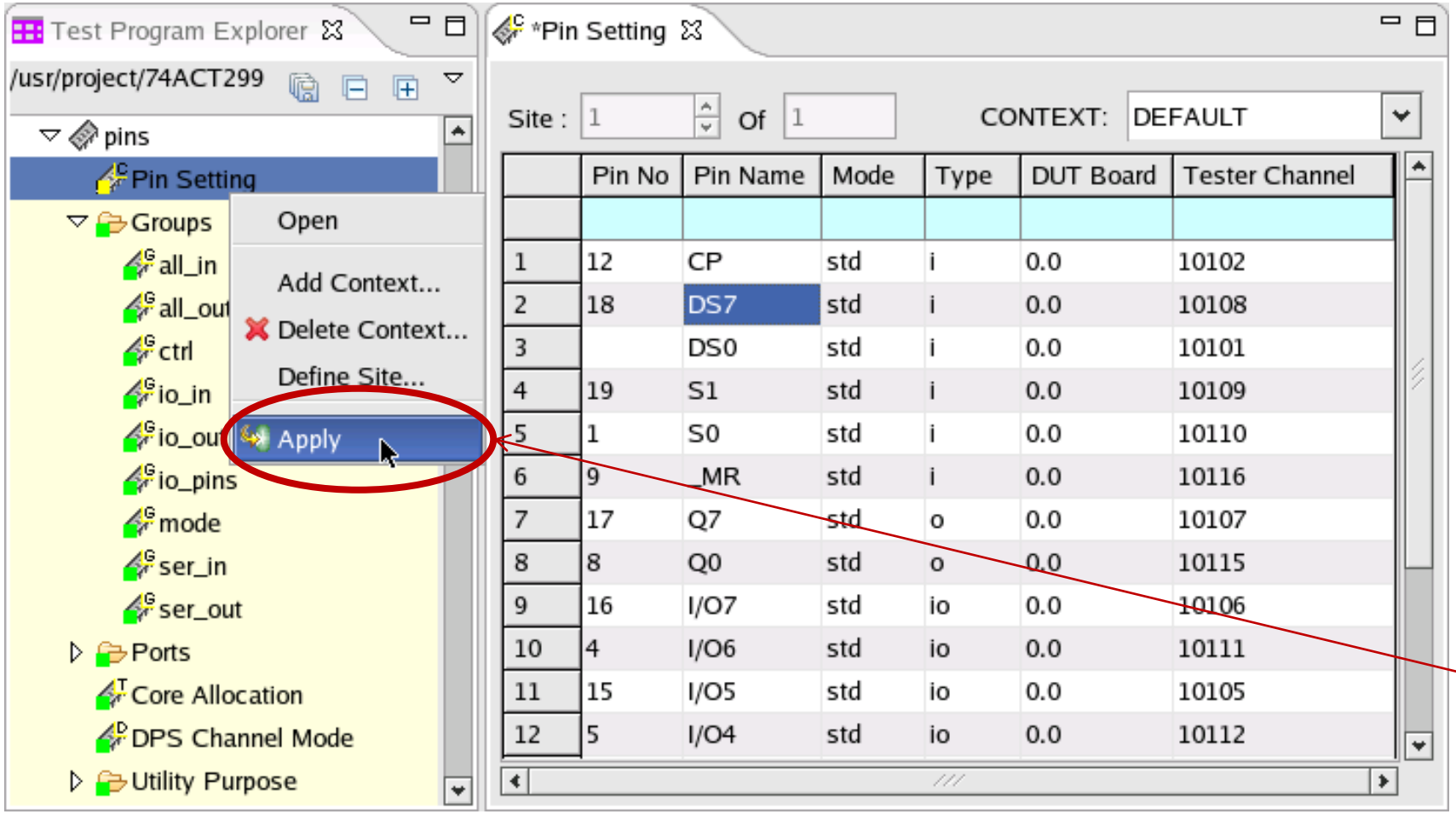
Site : 1 Of 1 CONTEXT: DEFAULT

	Pin No	Pin Name	Mode	Type	DUT Board	Tester Channel
1	12	CP	std	i	0.0	10102
2	11	DS0	std	i	0.0	10101
3	18	DS7	std	i	0.0	10108
4	7	I/O0	std	io	0.0	10114
5	13	I/O1	std	io	0.0	10103
6	6	I/O2	std	io	0.0	10113
7	14	I/O3	std	io	0.0	10104
8	5	I/O4	std	io	0.0	10112
9	15	I/O5	std	io	0.0	10105
10	4	I/O6	std	io	0.0	10111
11	16	I/O7	std	io	0.0	10106
12	8	Q0	std	o	0.0	10115
13	17	Q7	std	o	0.0	10107
14	1	S0	std	i	0.0	10110
15	19	S1	std	i	0.0	10109
16		Vcc		DPS+	0.0	DPS11
17	9	_MR	std	i	0.0	10116

Pin Type determines the parameters that will be defined

All following definitions (levels, timing, pattern) will be made using Pin Name

PIN SETTING IN SMARTEST

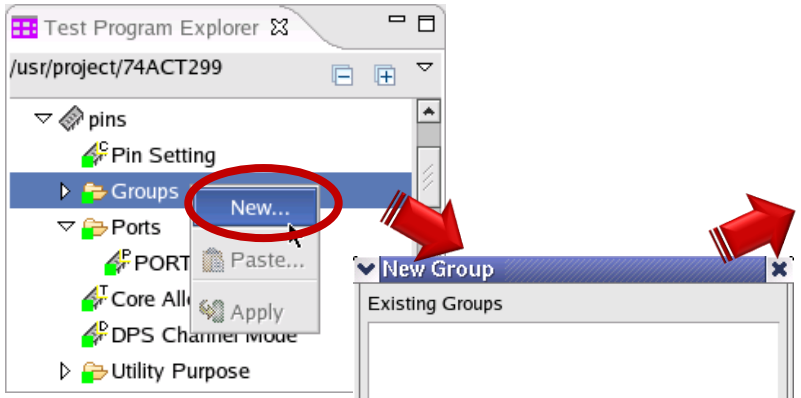


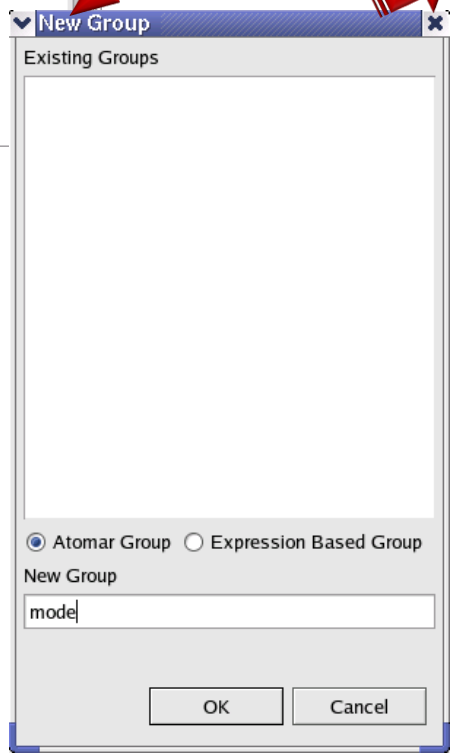
Error message if:
- test channel already used
- test channel unavailable

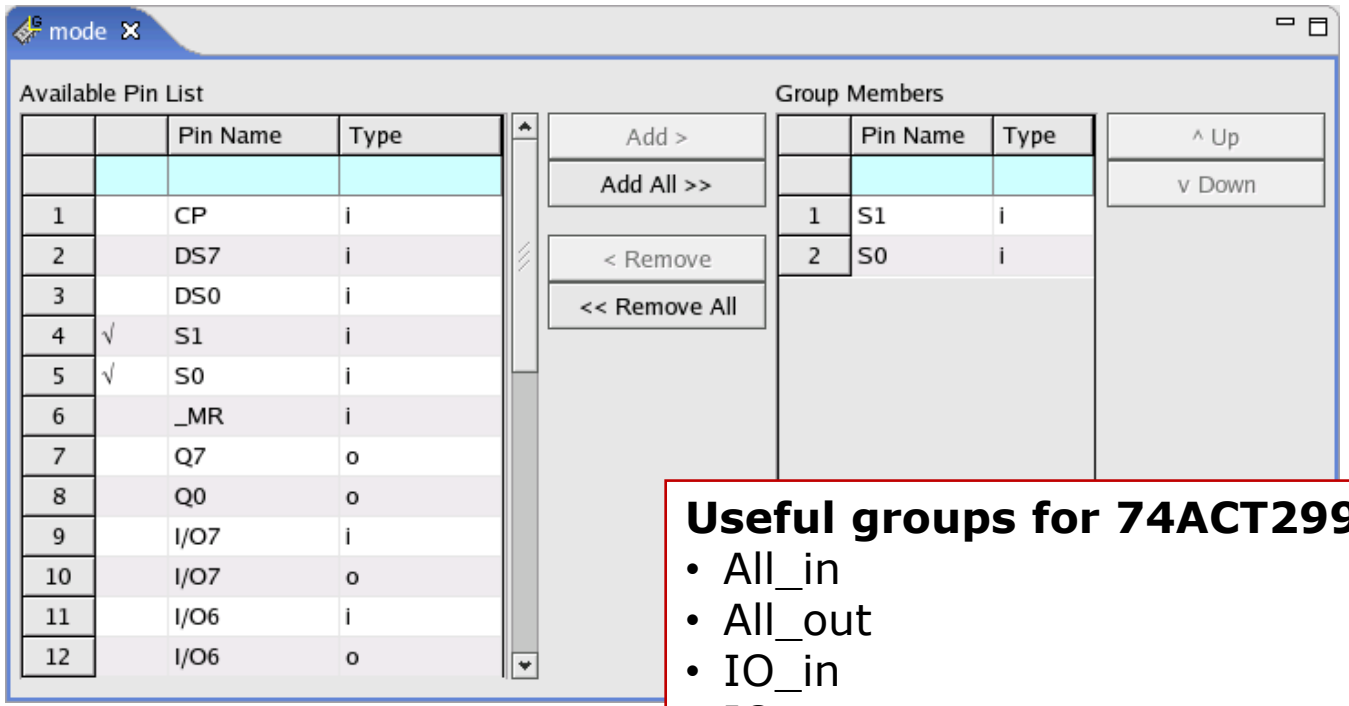
No error message if:
- test channel exists, even if the DUT pin is not connected to this channel

PIN SETTING IN SMARTEST

Defining Goups



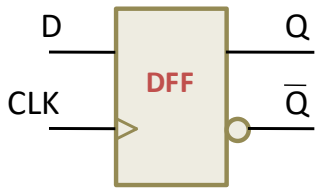




Useful groups for 74ACT299

- All_in
- All_out
- IO_in
- IO_out
- IO_pins
- Mode
- Ser_in
- Ser_out

EXAMPLE



LEVELS

Relaxed Levels

	Vil	Vih
D, CLK	0V	Vcc

	Vol	Voh
Q, Qb	Vcc/2 - 10% Vcc	Vcc/2 + 10% Vcc

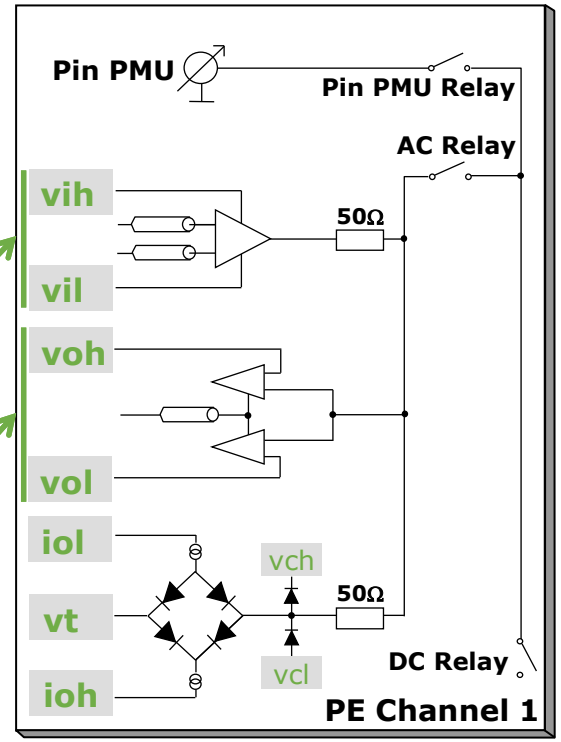
Equation Set

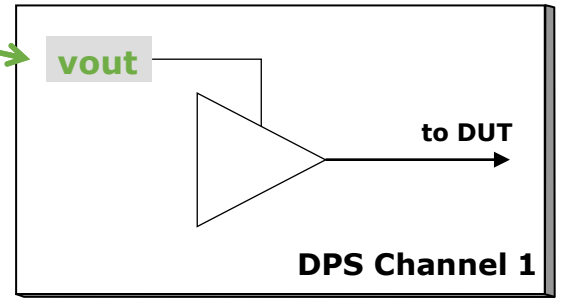
Supply pins
```
EQNSET 1 "Without specs & eqn"
DPSPINS Vcc
vout  = 5.0
```

Level Set

Input pins
```
LEVEL SET 1 "The only level set"
PINS  D, CLK
 vil   = 0
 vih   = 5.0
```

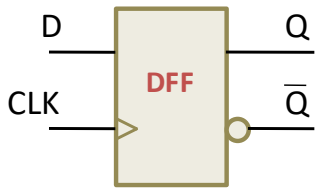
Output pins
```
PINS Q Qb
 vol  = 2.25
 voh = 2.75
```





LEVELS

EXAMPLE



VCC: Spec variable

Relaxed Levels

	Vil	Vih
D, CLK	0V	Vcc

	Vol	Voh
Q, Qb	Vcc/2 - 10% Vcc	Vcc/2 + 10% Vcc

```
EQNSET 1 "With specs & eqn"
DPSPINS Vcc
vout  = VCC

LEVEL SET 1 "The only level set"
PINS  D, CLK
 vil   = 0
 vih   = VCC

PINS Q Qb
 vol  = VCC/2 - 0.1 x VCC
 voh = VCC/2 + 0.1 x VCC
```

Equation Set

Supply pins

```
EQNSET 1 "Without specs & eqn"
DPSPINS Vcc
vout  = 5.0
```

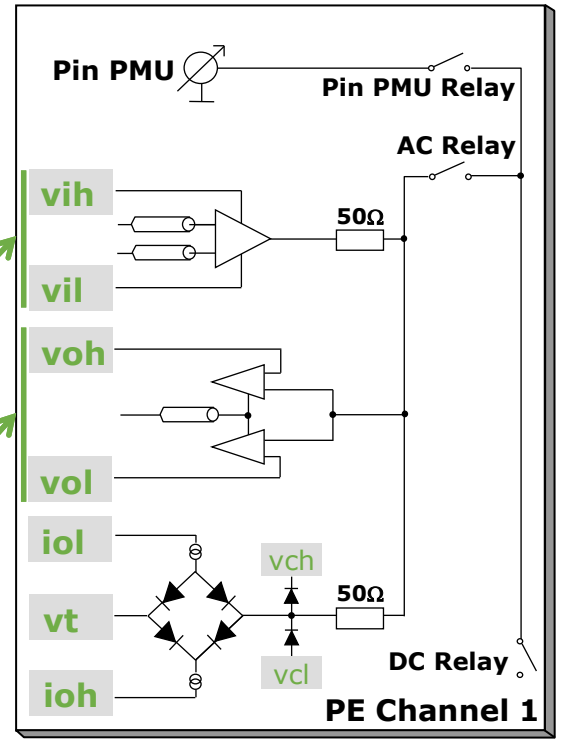
Level Set

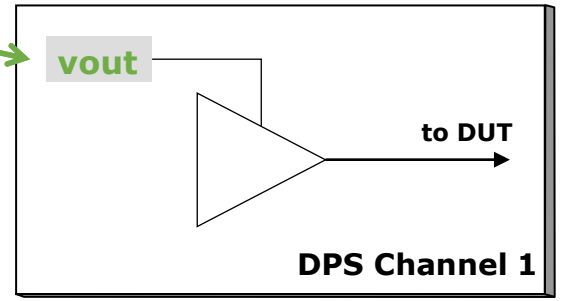
Input pins

```
LEVEL SET 1 "The only level set"
PINS  D, CLK
 vil   = 0
 vih   = 5.0
```

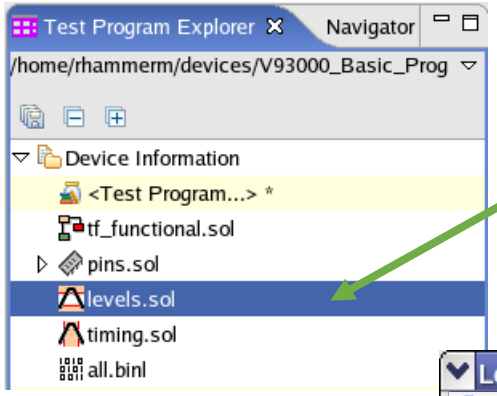
Output pins

```
PINS Q Qb
 vol  = 2.25
 voh = 2.75
```





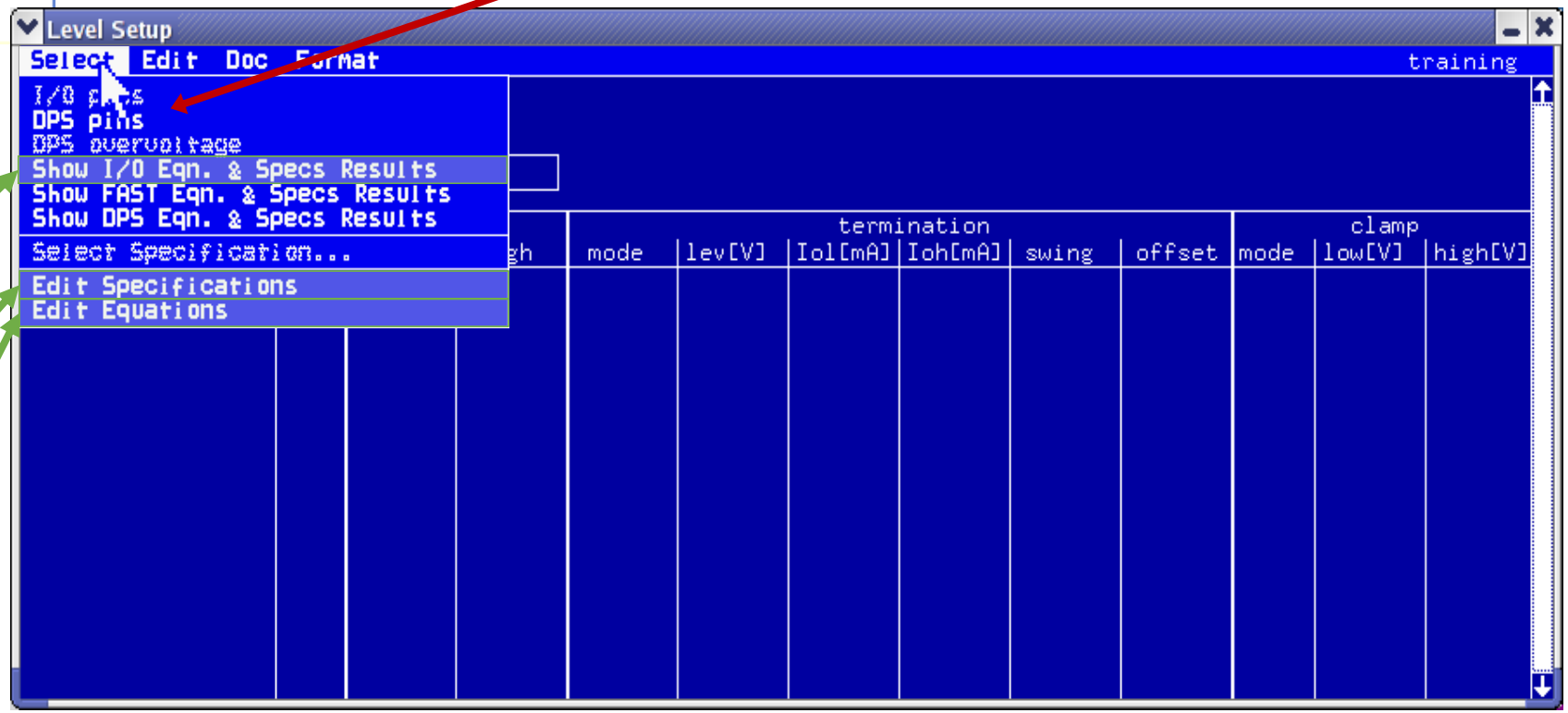
LEVEL SETTING IN SMARTEST



In the Test Program Explorer

1. **Load levels file**
2. **Open or Double-click on the levels item**

Switch between I/O pins & DPS pins



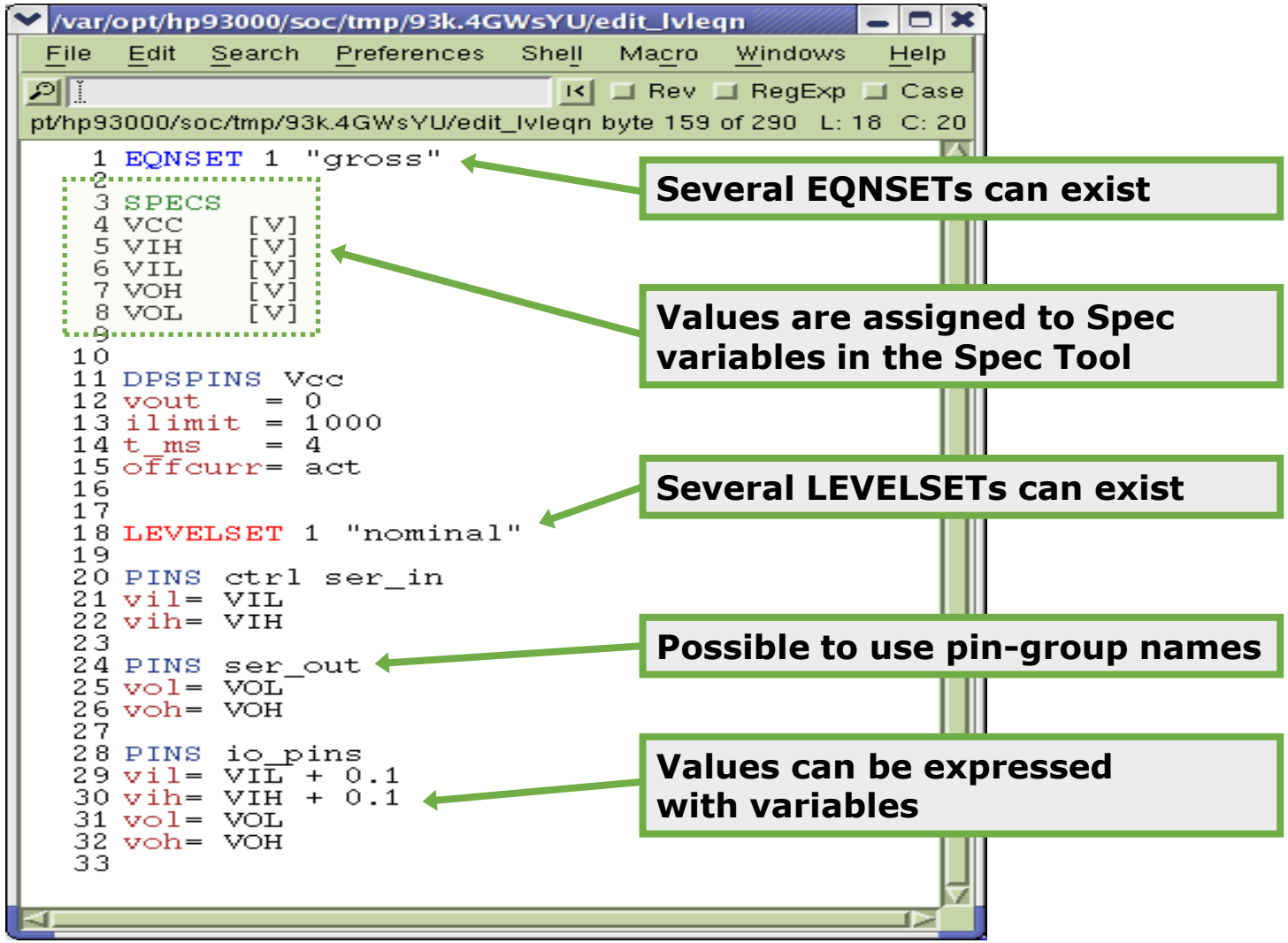
Show actual settings

Open SpecTool Window

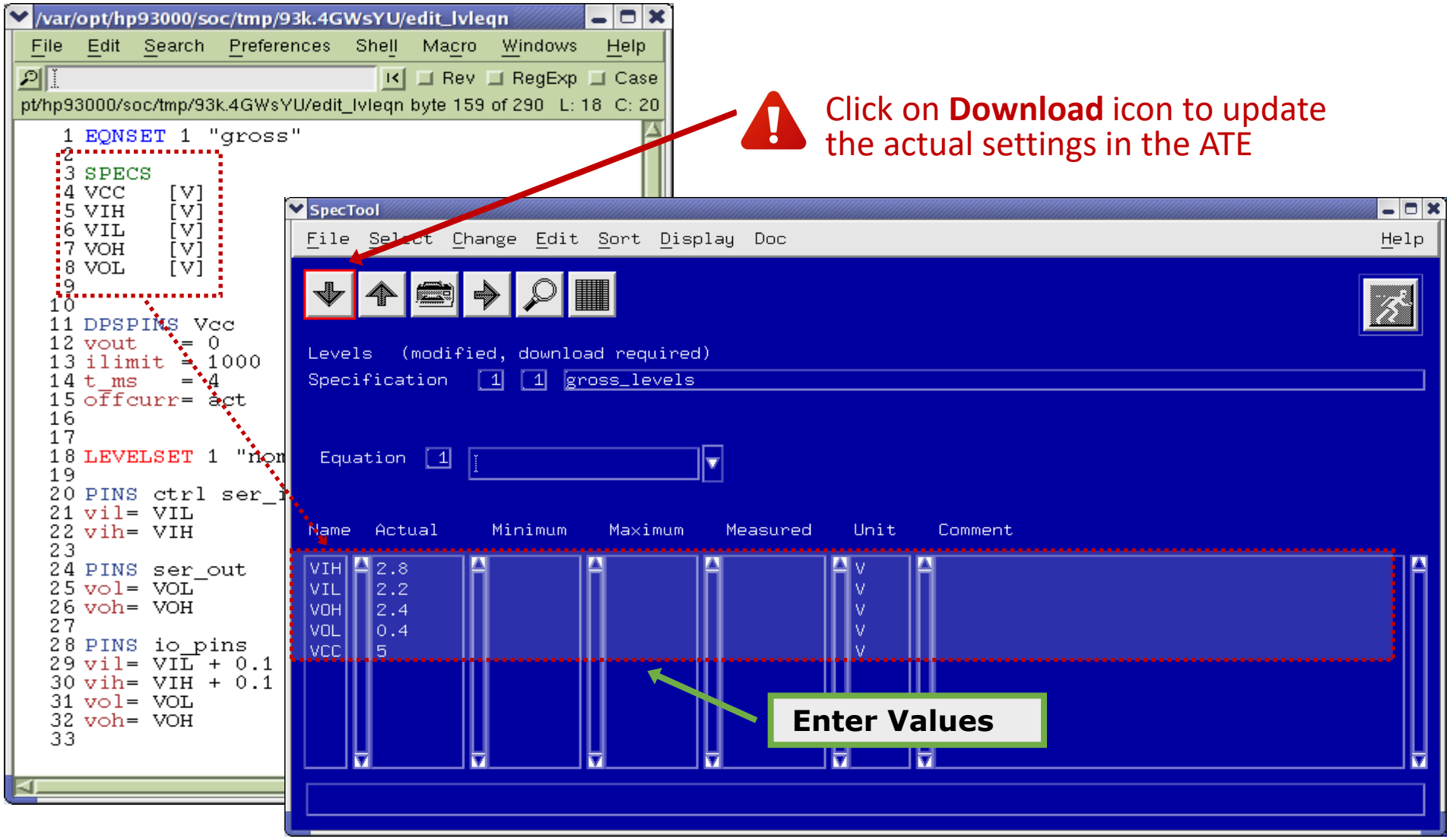
Open EQN SET Editor

LEVEL SETTING IN SMARTEST

LEVEL EQUATION SET EDITOR



LEVEL SETTING IN SMARTEST



LEVEL SPEC TOOL

LEVEL SETTING IN SMARTEST

Define a format to display pin groups instead of all individual pins

ACTUAL SETTINGS

"Show I/O Eqn. & Specs Results"

Level Setup

Select Edit Doc Format standard

Eqn# 2 Sps# 1 Lset# 1 of 3 Level no termination

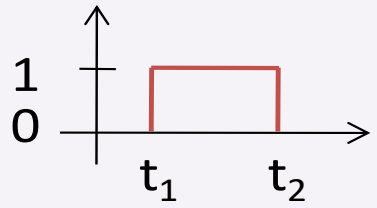
Specification Vcc = 4.5v Equation specs Fast Std

pin/group name	pin type	level[V] low	level[V] high	termination mode	termination lev[V]	termination Iol[mA]	termination Ioh[mA]	termination swing	termination offset	clamp mode	clamp low[V]	clamp high[V]
CP	i	0.000	4.250	off						off	-2.000	7.000
mode	i	0.000	4.250	off						off	-2.000	7.000
ser_in	i	0.000	4.250	off						off	-2.000	7.000
io_in	i	0.000	4.250									
io_out	o	2.200	2.300	off						off	-2.000	7.000
ser_out	o	2.200	2.300	off						off	-2.000	7.000

TIMING

- Concept
  - Define waveforms by associating actions to edges ➡ **Waveform Tables**
  - Specify tester period and position of edges ➡ **Timing Sets**

Waveform Tables



Timing Sets

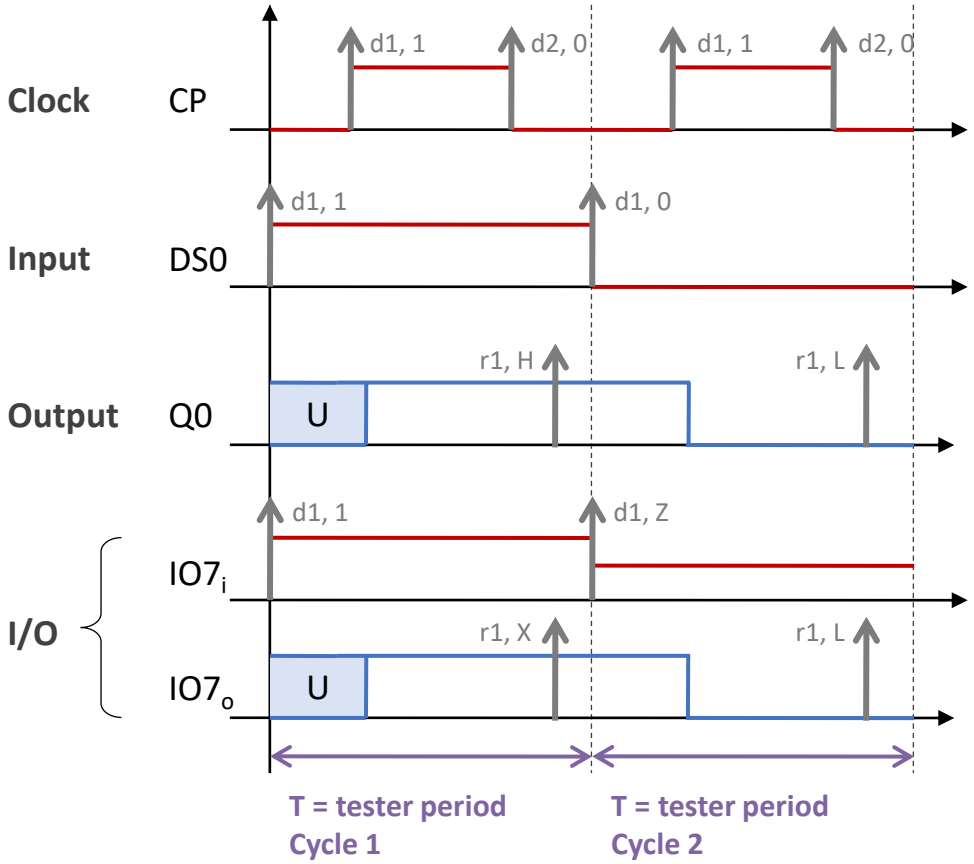
Tester timing resources per pin

- Input pins: 8 drive edges (d1, d2, …, d8)
- Output pins: 8 receive edges (r1, r2, …, r8)
- I/O pins: 8 drive edges + 8 receive edges

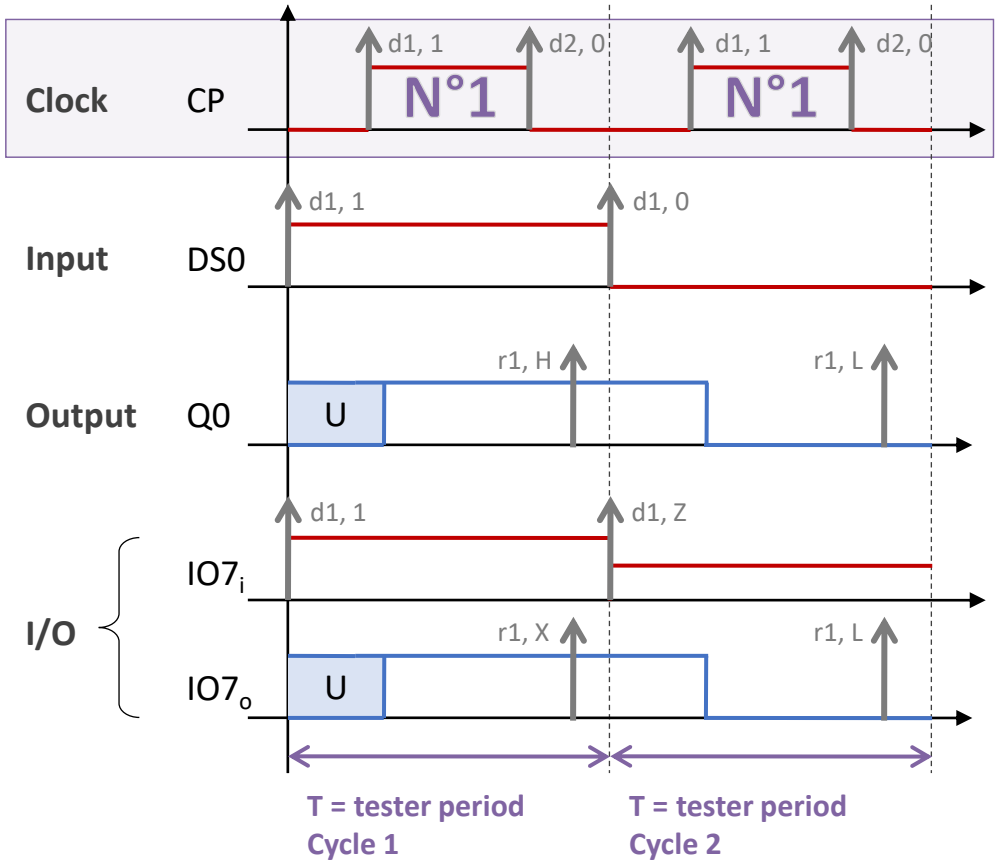
Actions

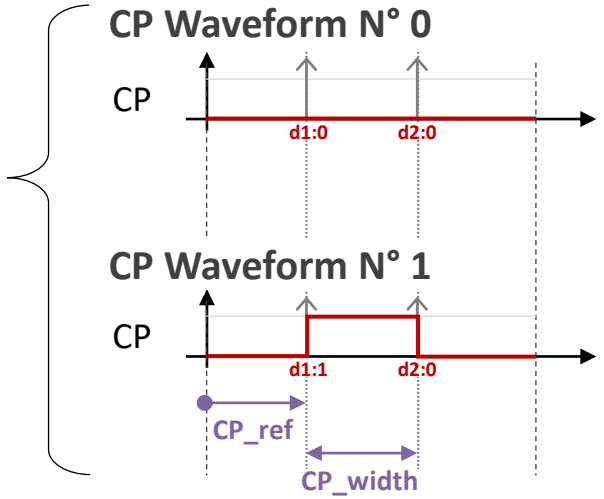
- Drive actions
  - 0: Drive '0'
  - 1: Drive '1'
  - Z: High impedance
  - N: No action
- Receive actions *(edges)*
  - L: Compare to 'Low'
  - H: Compare to 'High'
  - M: Compare to 'Intermediate'
  - X: Don't care

TIMING PROGRAMMING



TIMING PROGRAMMING





Programming – Clock

Waveforms

N° 0 - d1:0 d2:0 *(Clock Inactive)*

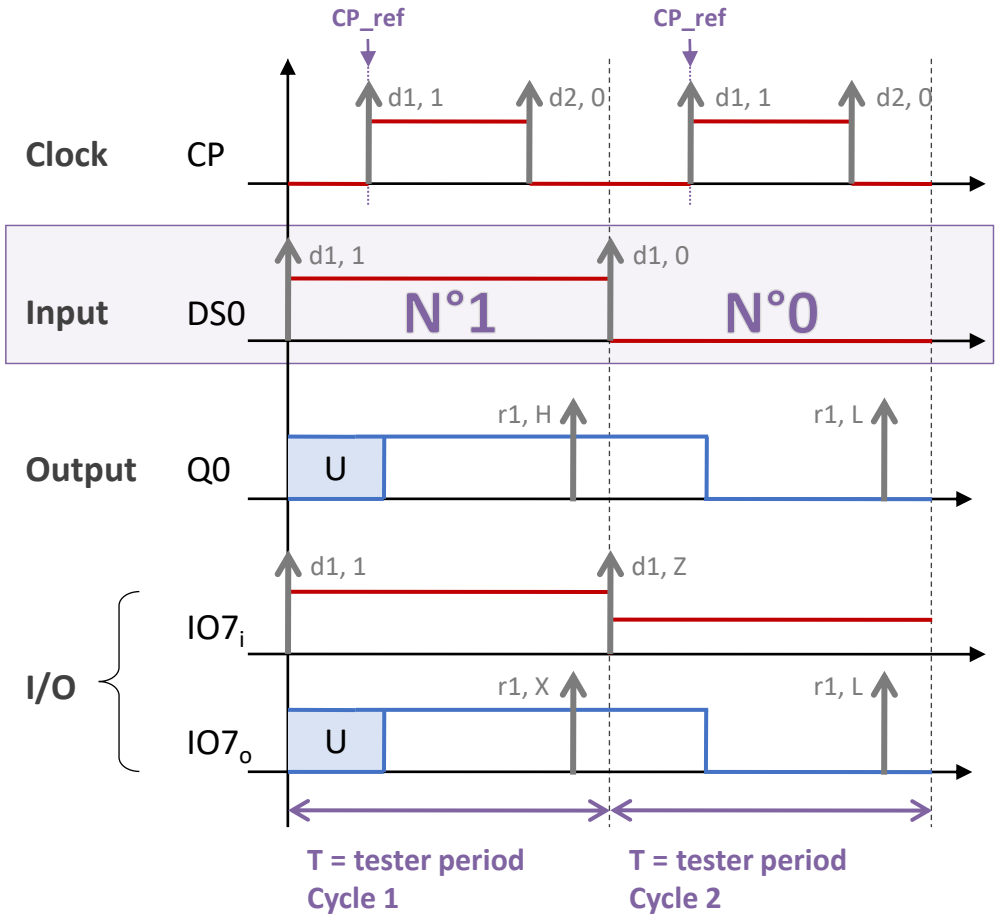
N° 1 - d1:1 d2:0

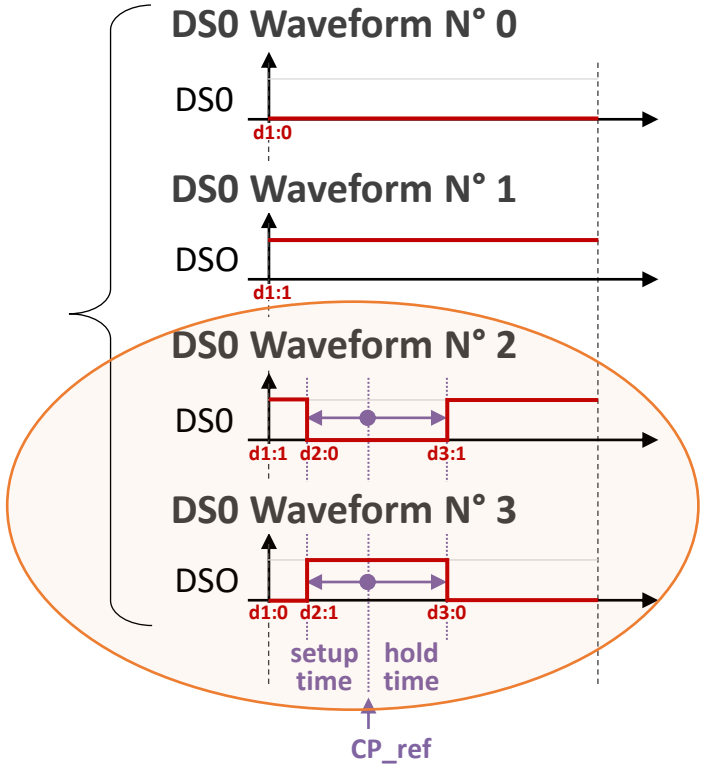
Edges Position

d1: CP_ref

d2: CP_ref + CP_width or after

TIMING PROGRAMMING





Programming – Input

Waveforms

N° 0 - d1:0
N° 1 - d1:1
} *DNRZ format*

N° 2 - d1:1 d2:0 d3:1
N° 3 - d1:0 d2:1 d3:0
} *SBC format*

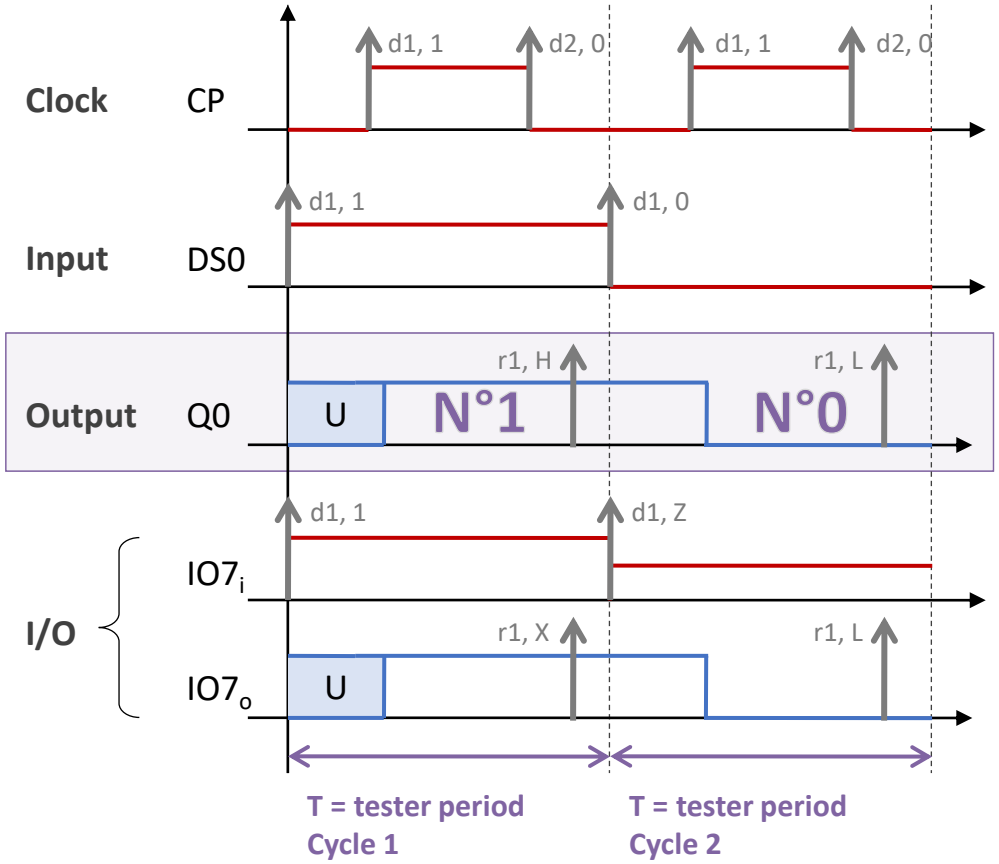
Edges Position

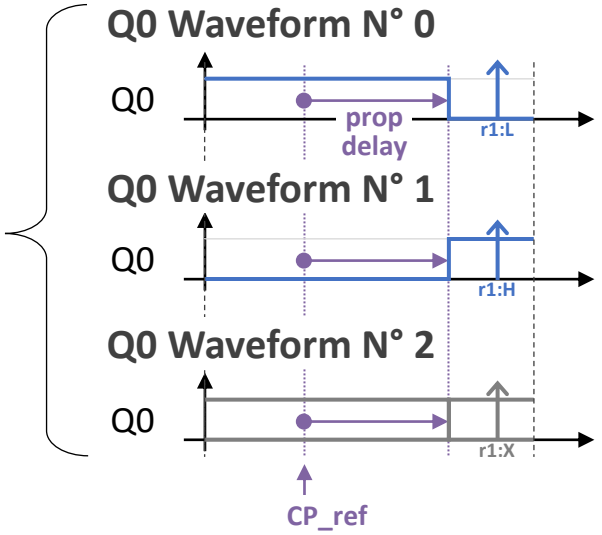
d1: 0ns
d2: **CP_ref - setup_time** or before
d3: **CP_ref + hold_time** or after

WF definition to handle verification of setup & hold times:

- SBC format (3 edges)

TIMING PROGRAMMING





Programming – Output

Waveforms

N° 0 - r1:L

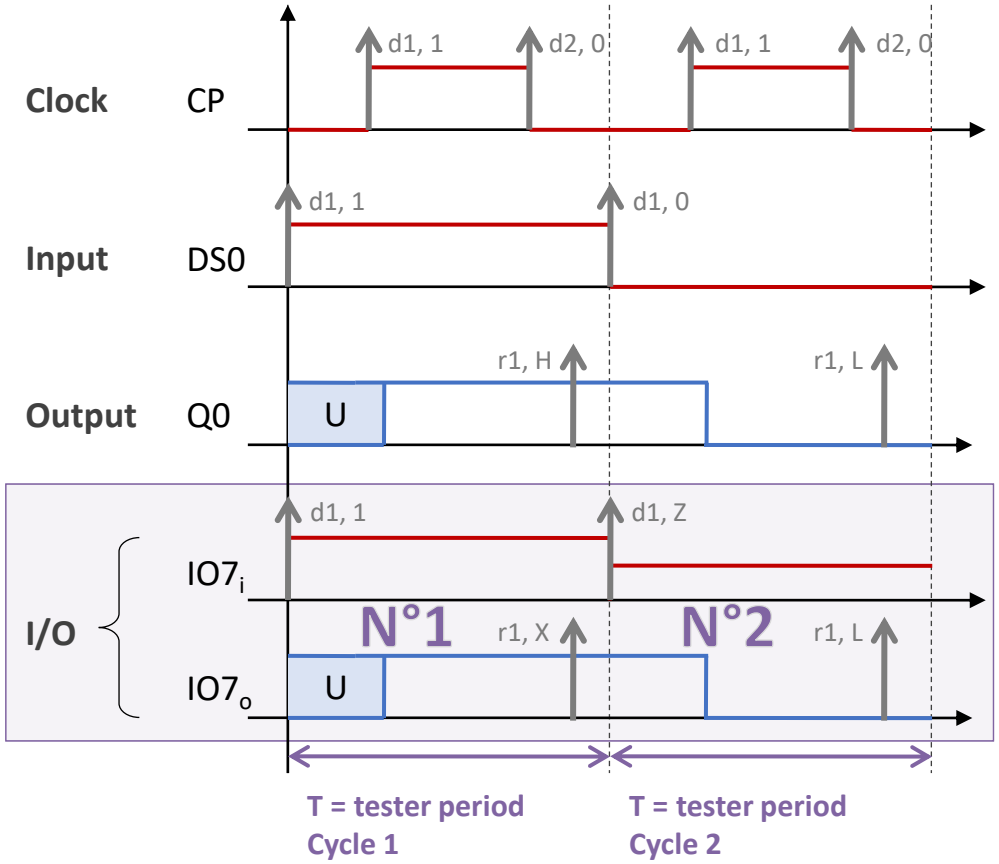
N° 1 - r1:H

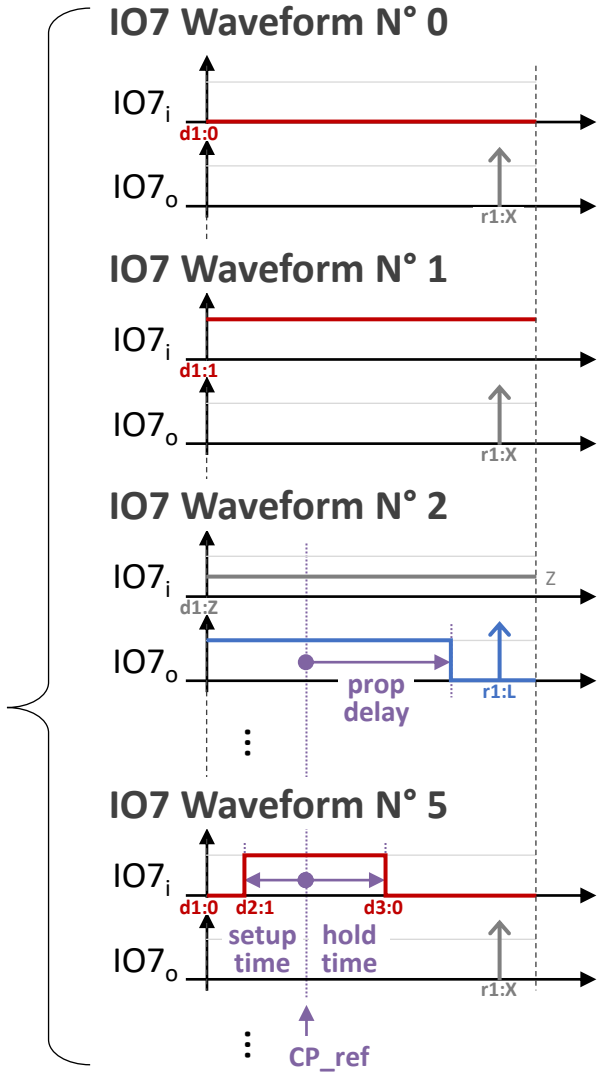
N° 2 - r1:X

Edges Position

r1: CP_ref + prop_delay or after

TIMING PROGRAMMING





Programming – I/O Pins

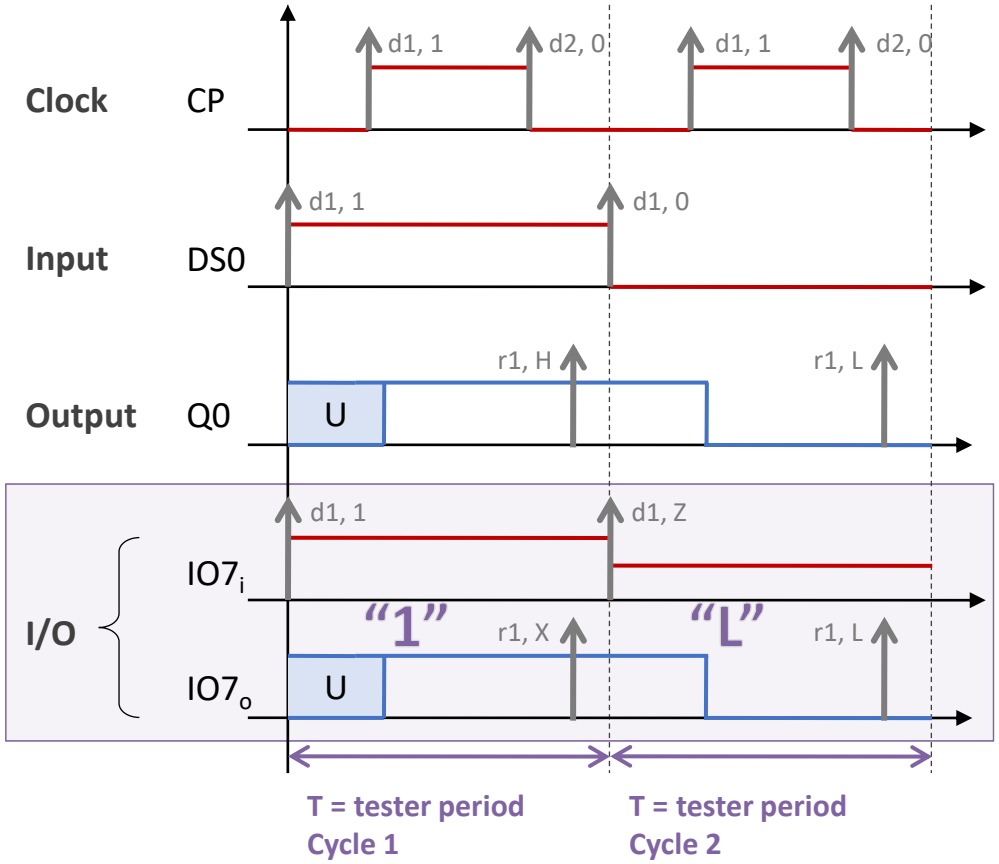
Waveforms

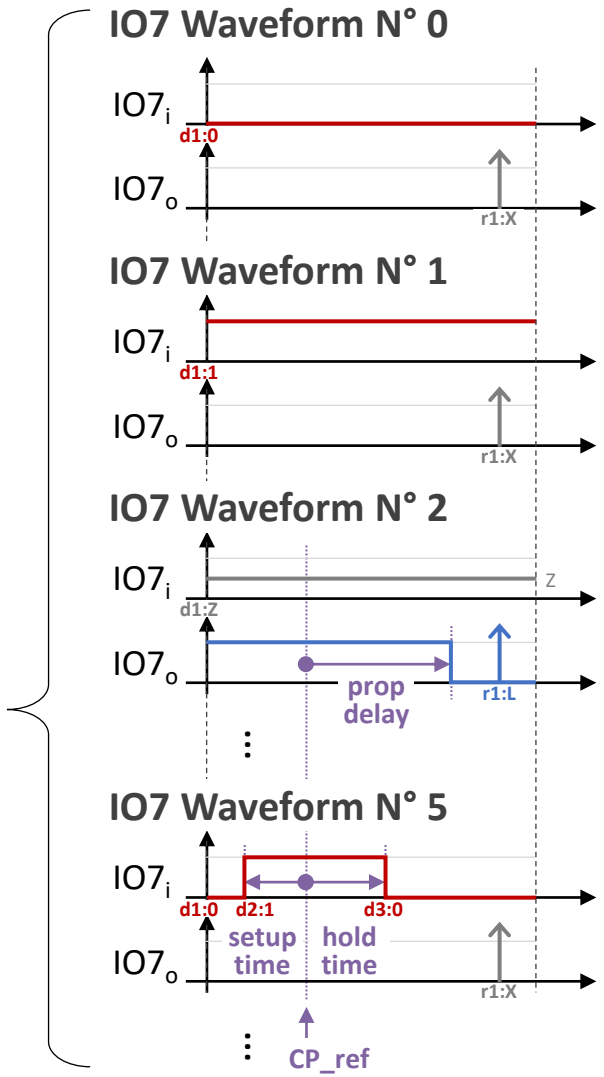
N° 0 - d1:0 r1:X
N° 1 - d1:1 r1:X
N° 2 - d1:Z r1:L
N° 3 - d1:Z r1:H
N° 4 - d1:Z r1:X
N° 5 - d1:0 d2:1 d3:0 r1:X
N° 6 - d1:1 d2:0 d3:1 r1:X
…

Edges Position

d1: 0ns
d2: CP_ref - setup_time or before
d3: CP_ref + hold_time or after
r1: CP_ref + prop_delay or after

TIMING PROGRAMMING





Waveform Name

Programming – I/O Pins

Waveforms

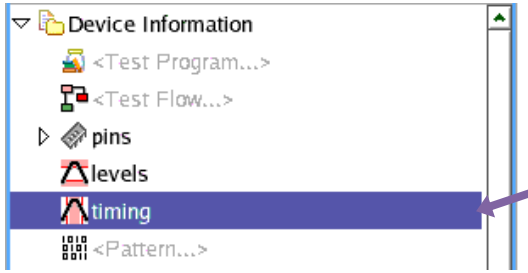
	Dev Cycle
N° 0 - d1:0 r1:X	"0"
N° 1 - d1:1 r1:X	"1"
N° 2 - d1:Z r1:L	"L"
N° 3 - d1:Z r1:H	"H"
N° 4 - d1:Z r1:X	"X"
N° 5 - d1:0 d2:1 d3:0 r1:X	"SBC_1"
N° 6 - d1:1 d2:0 d3:1 r1:X	"SBC_0"

…

Edges Position

d1: 0ns
d2: CP_ref - setup_time or before
d3: CP_ref + hold_time or after
r1: CP_ref + prop_delay or after

TIMING SETTING IN SMARTEST



In the Test Program Explorer

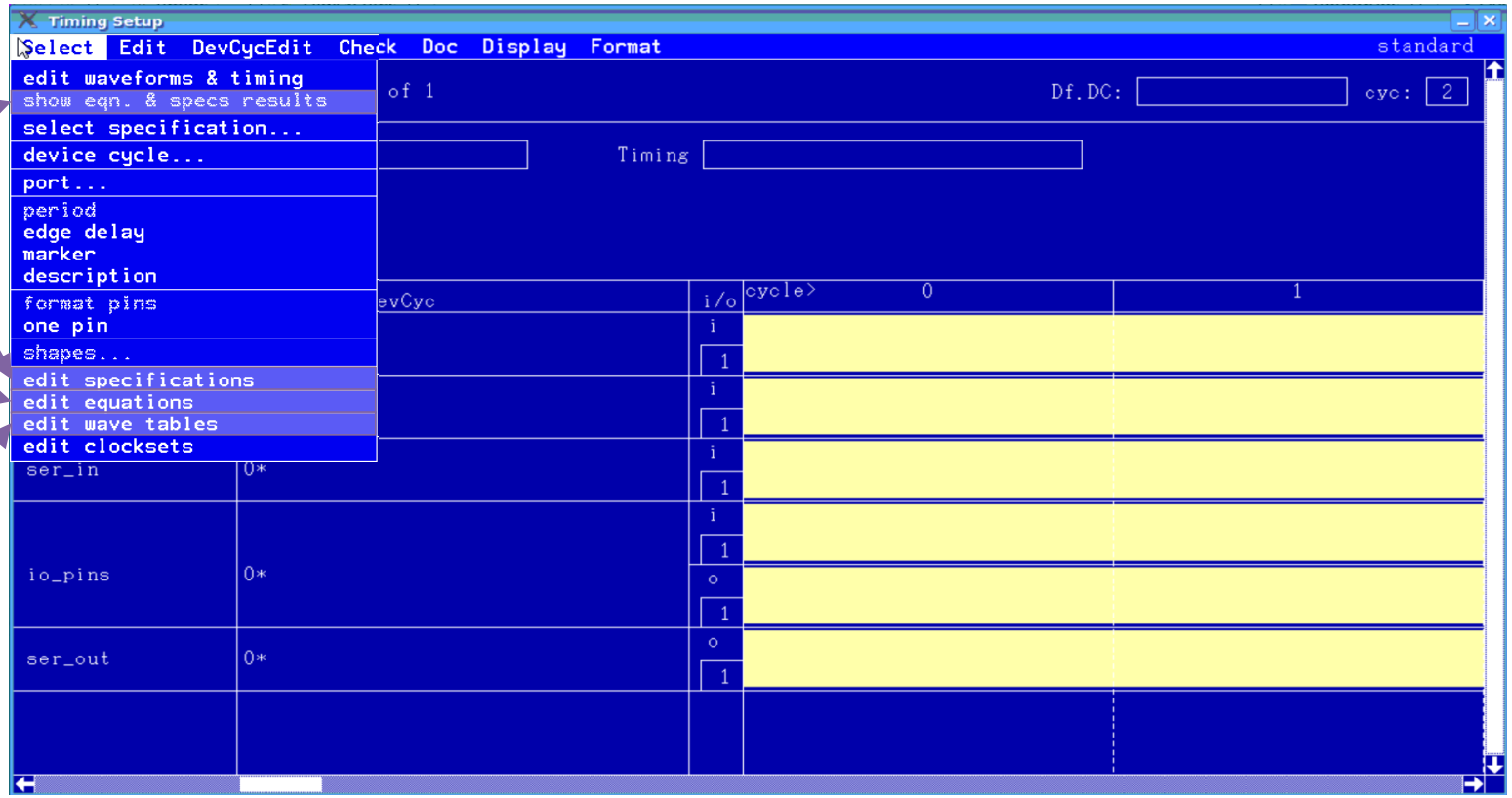
1. **Load timing file**
2. **Open or Double-click on the timing item**

Visualize Waveforms

Open SpecTool Window

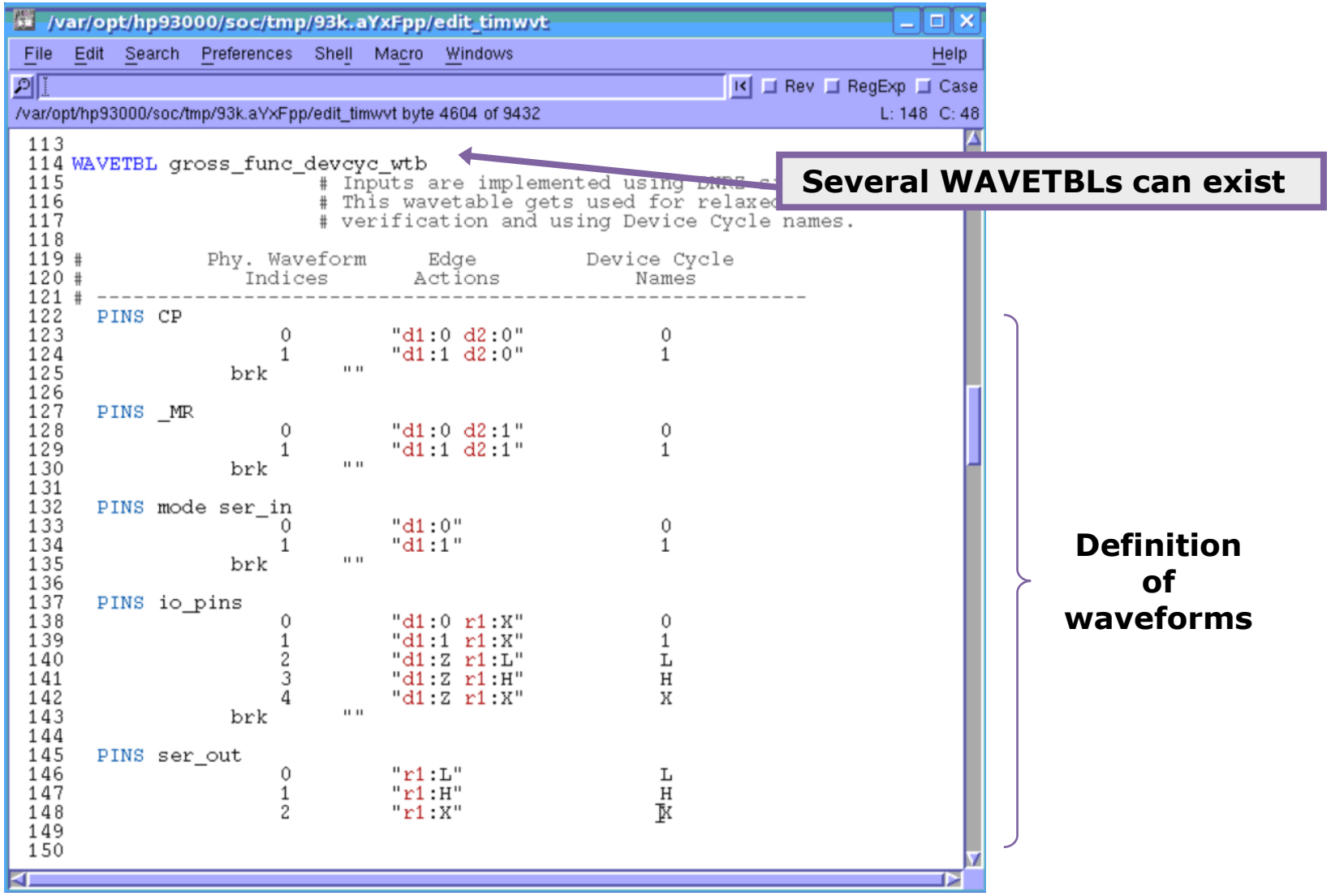
Open EQN SET Editor

Open WAVETABLE Editor



TIMING SETTING IN SMARTEST

WAVETABLE EDITOR



Several WAVETBLs can exist

Definition of waveforms

TIMING SETTING IN SMARTEST

TIMING EQUATION SET EDITOR

/var/opt/hp93000/soc/tmp/93k.sVSlr8/edit_timeqn

File Edit Search Preferences Shell Macro Windows Help

Find: Rev RegExp Case

/var/opt/hp93000/soc/tmp/93k.sVSlr8/edit_timeqn 2053 bytes

```
63
64  EQNSET 2 "spec_search_eqn"
65
66  SPECS
67 #-----------------------
68 #   Spec          Unit
69 # variables
70 #-----------------------
71
72  f               [MHz]
73  ts_Sx_CP        [ns]
74  th_CP_Sx        [ns]
75  ts_IOx_CP       [ns]
76  th_CP_IOx       [ns]
77  ts_DSx_CP       [ns]
78  th_CP_DSx       [ns]
79  tw_CP           [ns]
80  tw_MR           [ns]
81  trec_MR_CP      [ns]
82  tpd_CP_Qx       [ns]
83  tpd_CP_IOx      [ns]
84
85  EQUATIONS
86
87  p = 1/f*1000
88  CP_ref = p/2
89  ComplDelay = 2
90
91  TIMINGSET 1 "std"
92
93   period = p
94
95     PINS CP
96      d1 = CP_ref
97      d2 = CP_ref + tw_CP
98
```

Several EQNSETs can exist

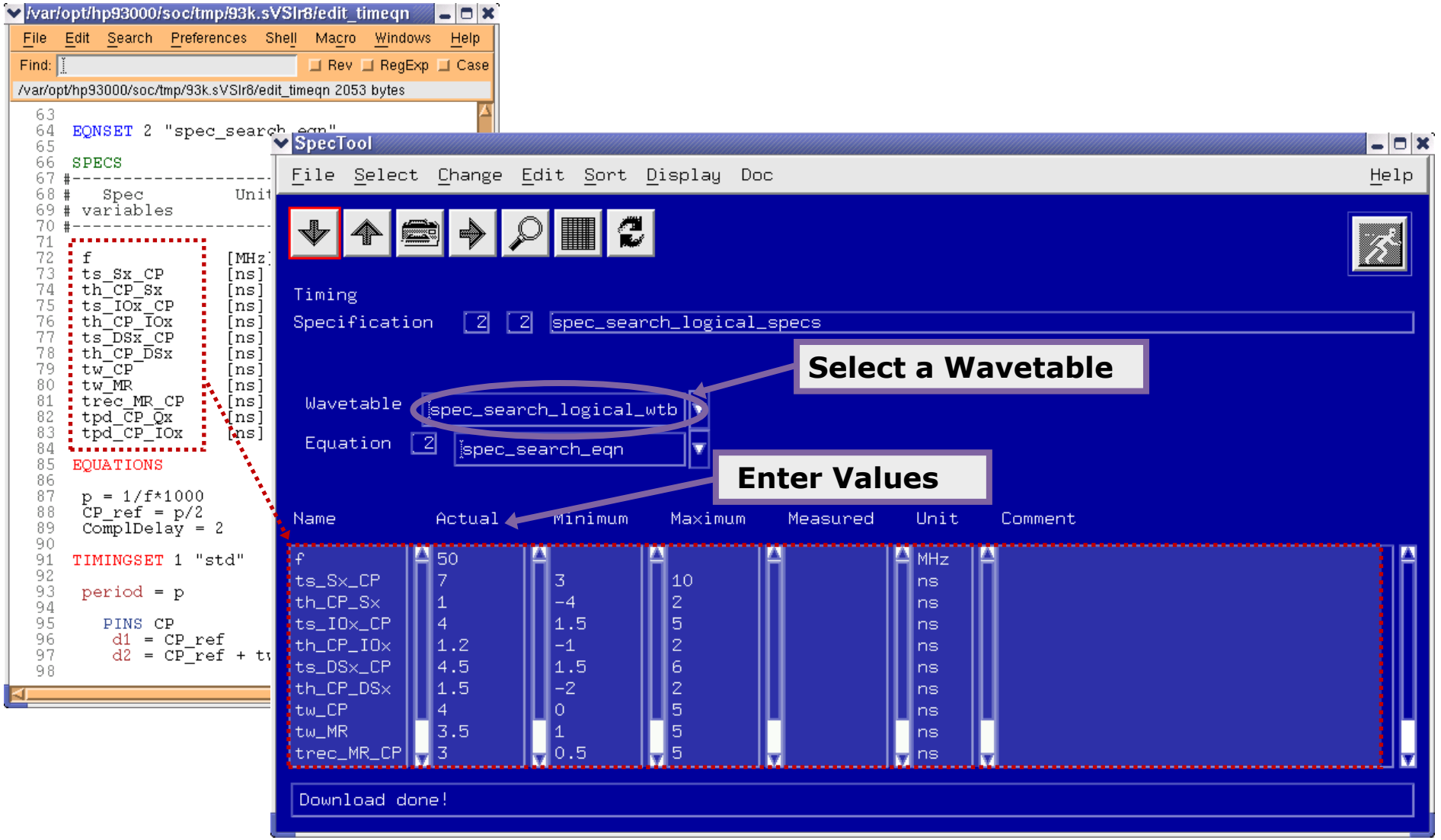
Values are assigned to Spec variables in the Spec Tool

Additional variables can be defined with equations that use Spec variables

Several TIMINGSETs can exist

Values can be expressed with variables

TIMING SETTING IN SMARTEST

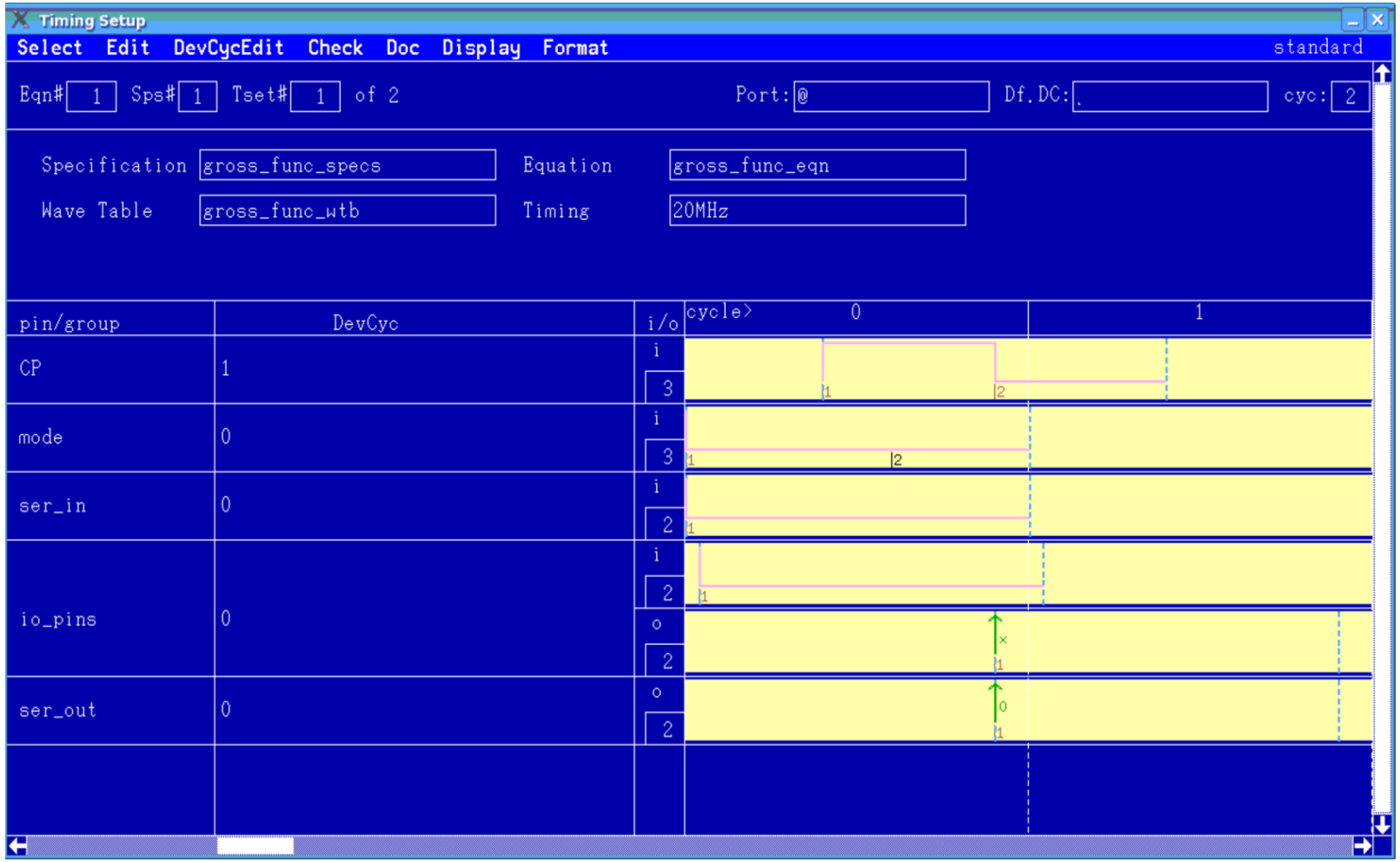


TIMING SPEC TOOL

TIMING SETTING IN SMARTEST

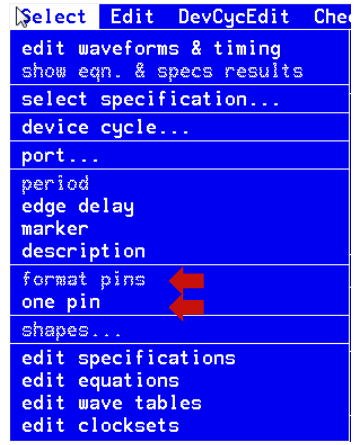
Waveform Visualization

"Show eqn.
& Specs Results"



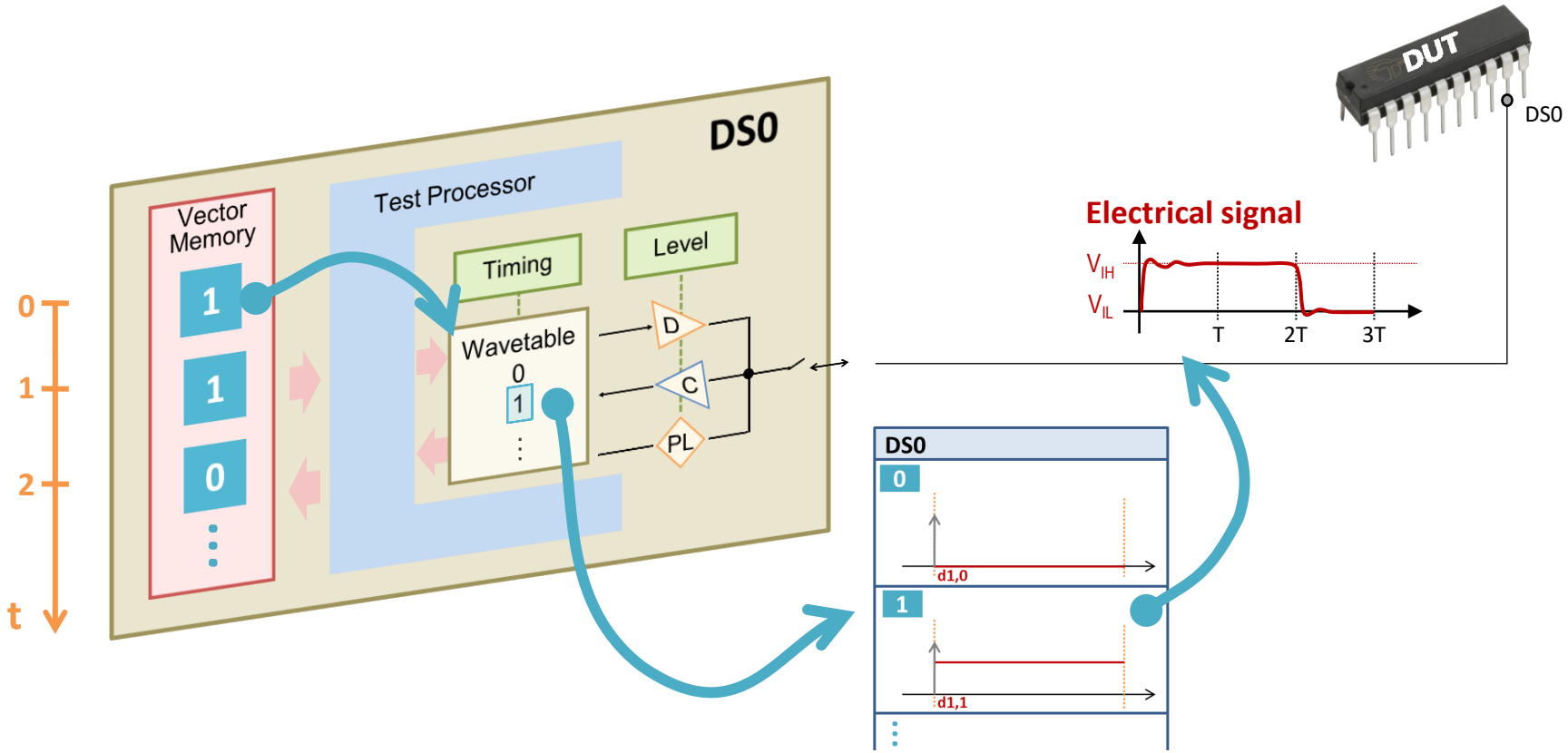
View with "**format pins**" active, i.e. only one waveform displayed for each pin or pin group

To see all waveforms defined for a given pin or pin group, click on the name of a pin or pin group and choose "**one pin**"



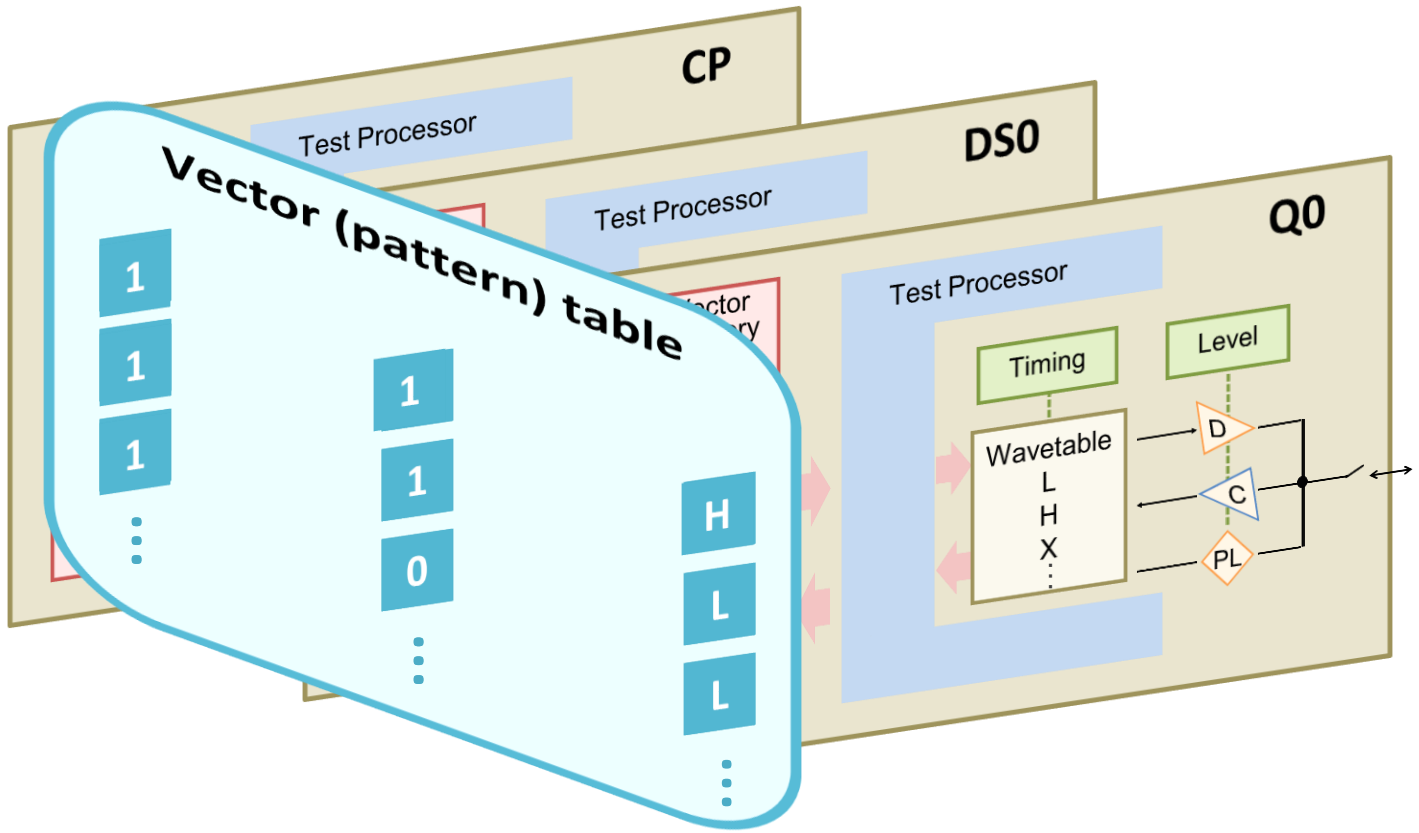
PATTERN

- Principle
  - Sequence of waveform indexes/names that will be “played” by the test processor



PATTERN

- Principle
  - Sequence of waveform indexes/names that will be “played” by the test processor

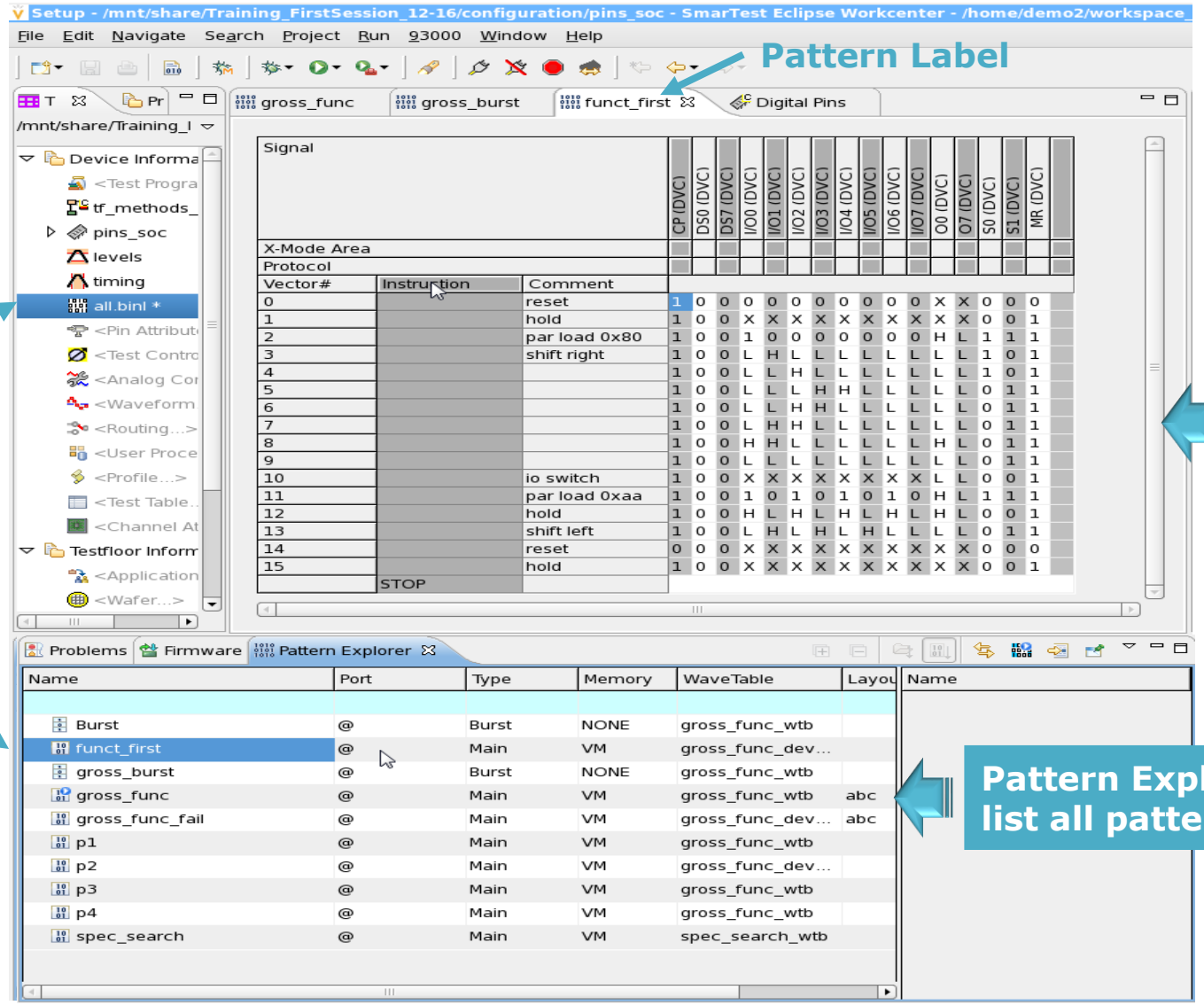


- Data in the pattern table do not directly correspond to a logic value but refer to a waveform index or name
- Pattern cannot be defined before timing (waveforms must exist before referring to them)

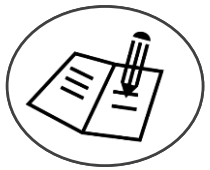
PATTERN TOOL IN SMARTEST

1. In the Test Program Explorer, double-click on the pattern item

2. In the Pattern Explorer, double-click on one pattern

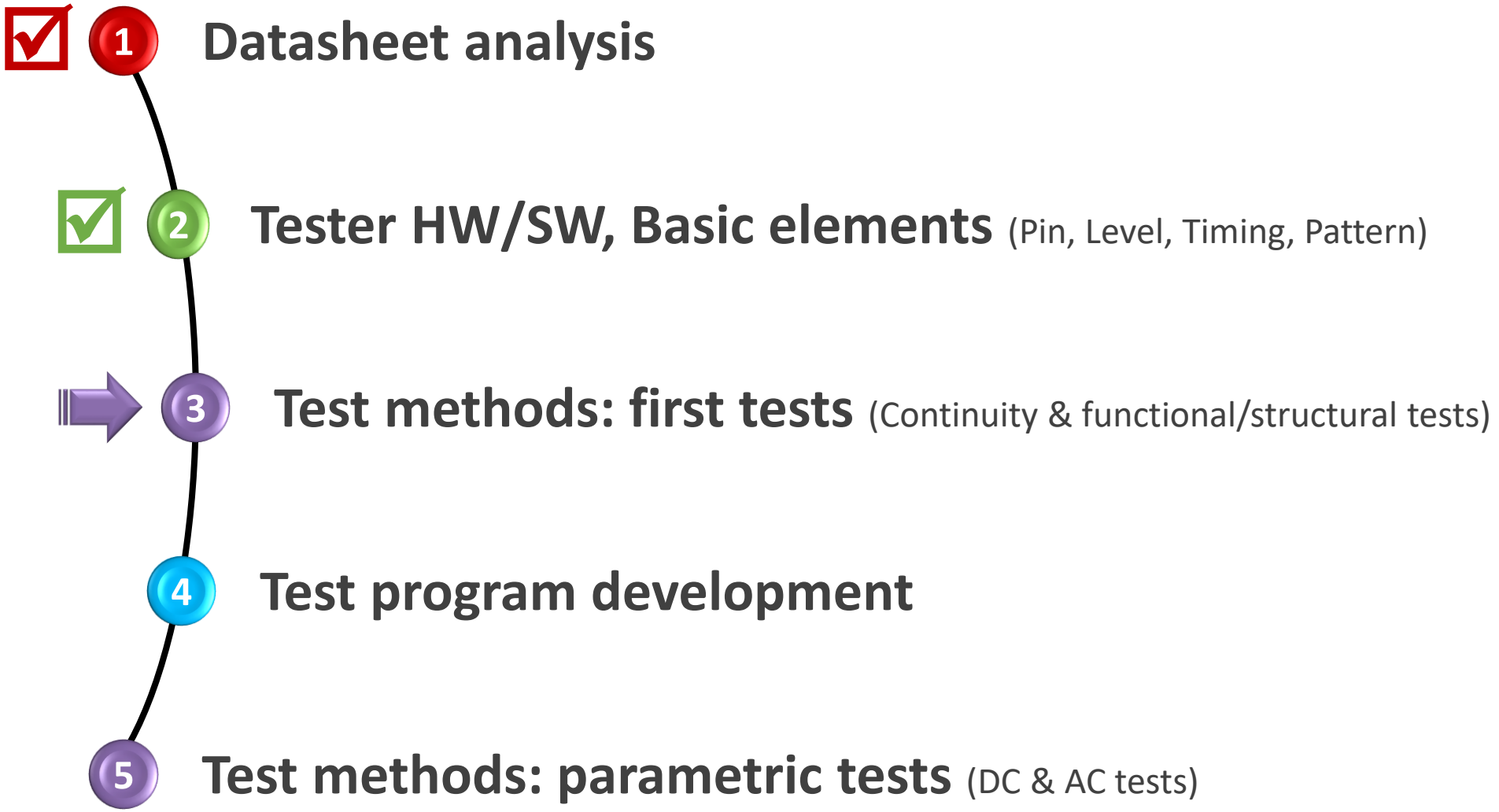


2



Lab & Exercises:
First Steps with SmarTest - Part 2

LEARNING STEPS

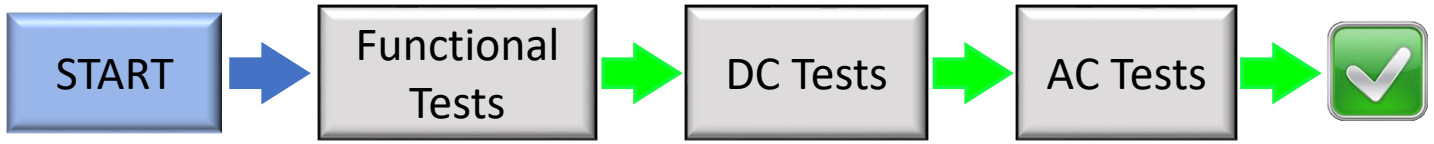


PART 3

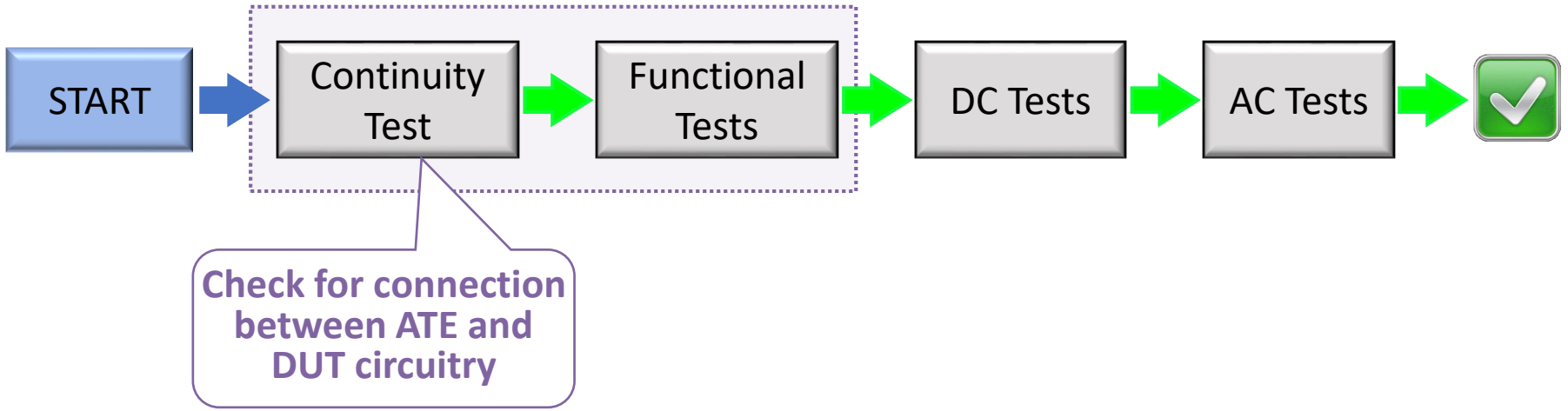
- Continuity Test
- Functional/Structural Tests

3 TEST METHODS: FIRST TESTS

- Test Flow planned from Datasheet Analysis



- Actual Production Test Flow

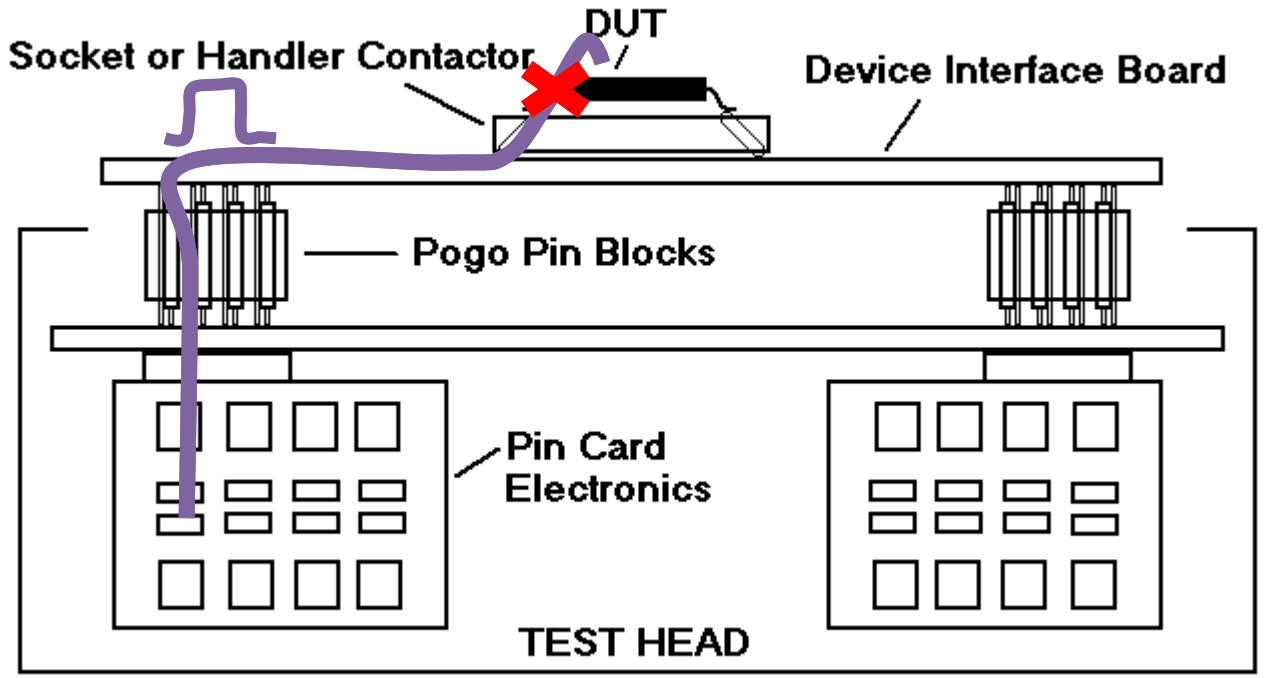


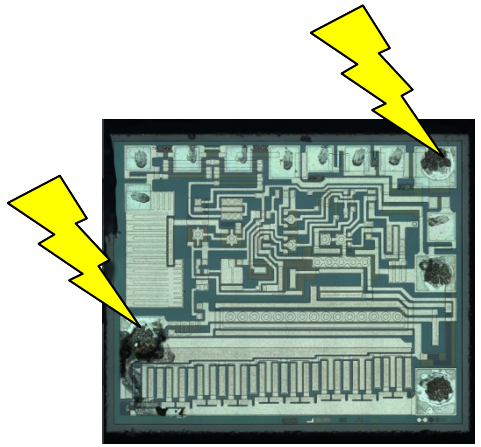
3 Test Methods: First Tests

Continuity Test

(also called “Open/Short Test” or “Contact Test”)

- Purpose
  - Verify the connection between ATE and DUT pins (no open)
  - Verify that no DUT pin is shorted to power/ground





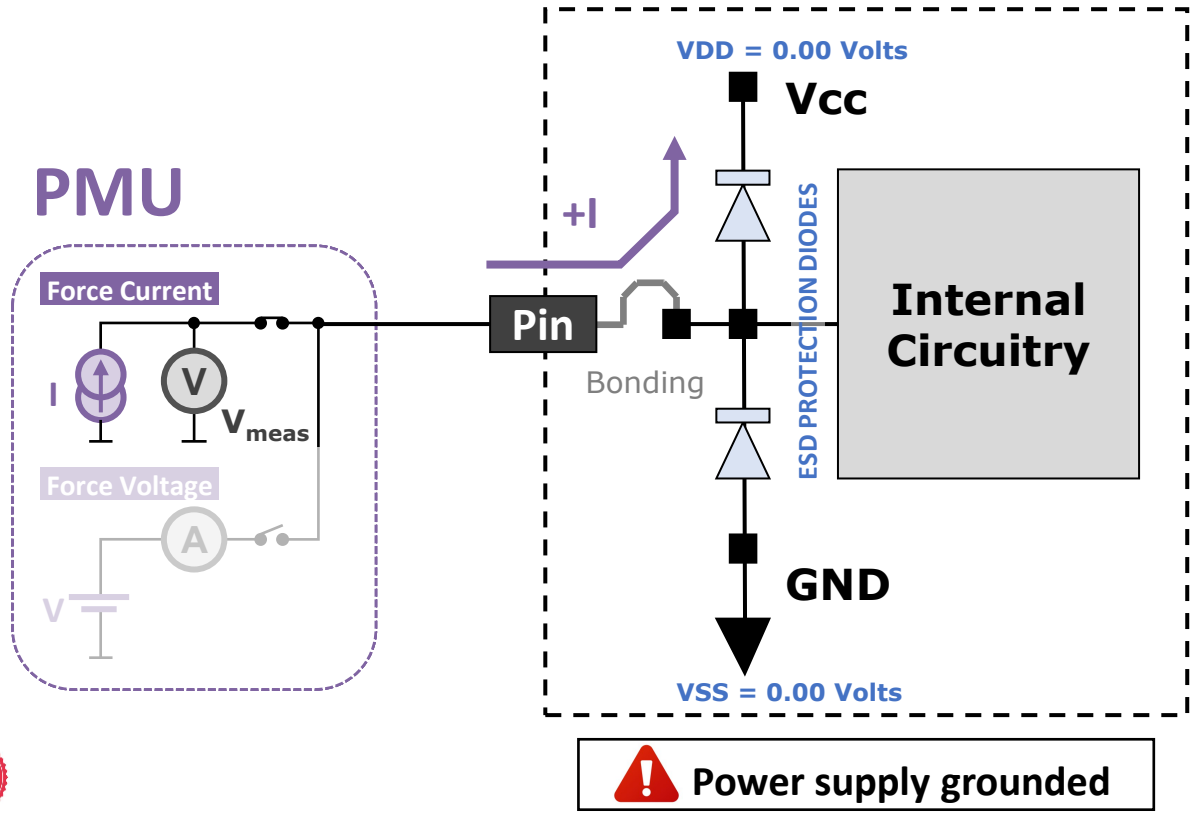
No ESD damage

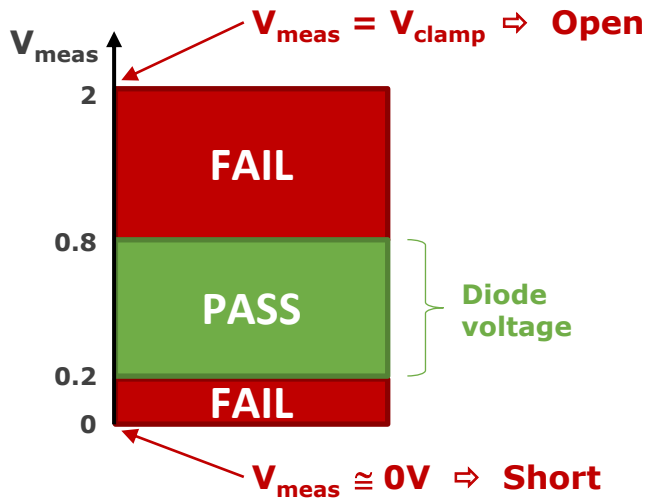
3 TEST METHODS: FIRST TESTS

CONTINUITY TEST

(also called “Open/Short Test” or “Contact Test”)

- Principle
  - **Force I & Measure V**: resulting voltage should be a <u>diode voltage</u> (ESD protection diodes)



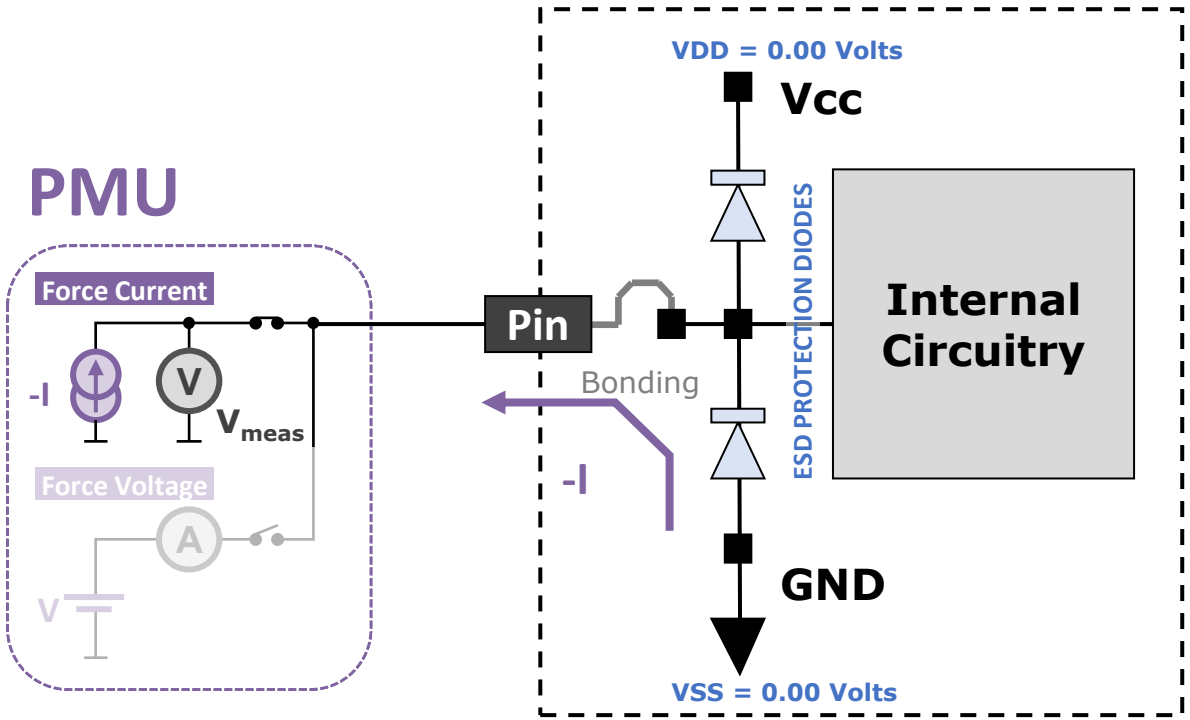


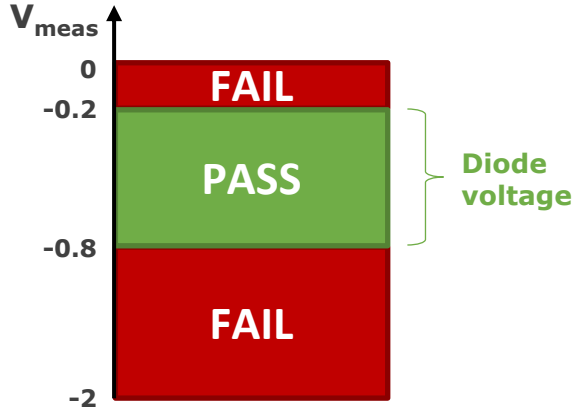
3 Test Methods: First Tests

Continuity Test

(also called “Open/Short Test” or “Contact Test”)

- Principle
  - **Force I & Measure V**: resulting voltage should be a <u>diode voltage</u> (ESD protection diodes)





Both polarities

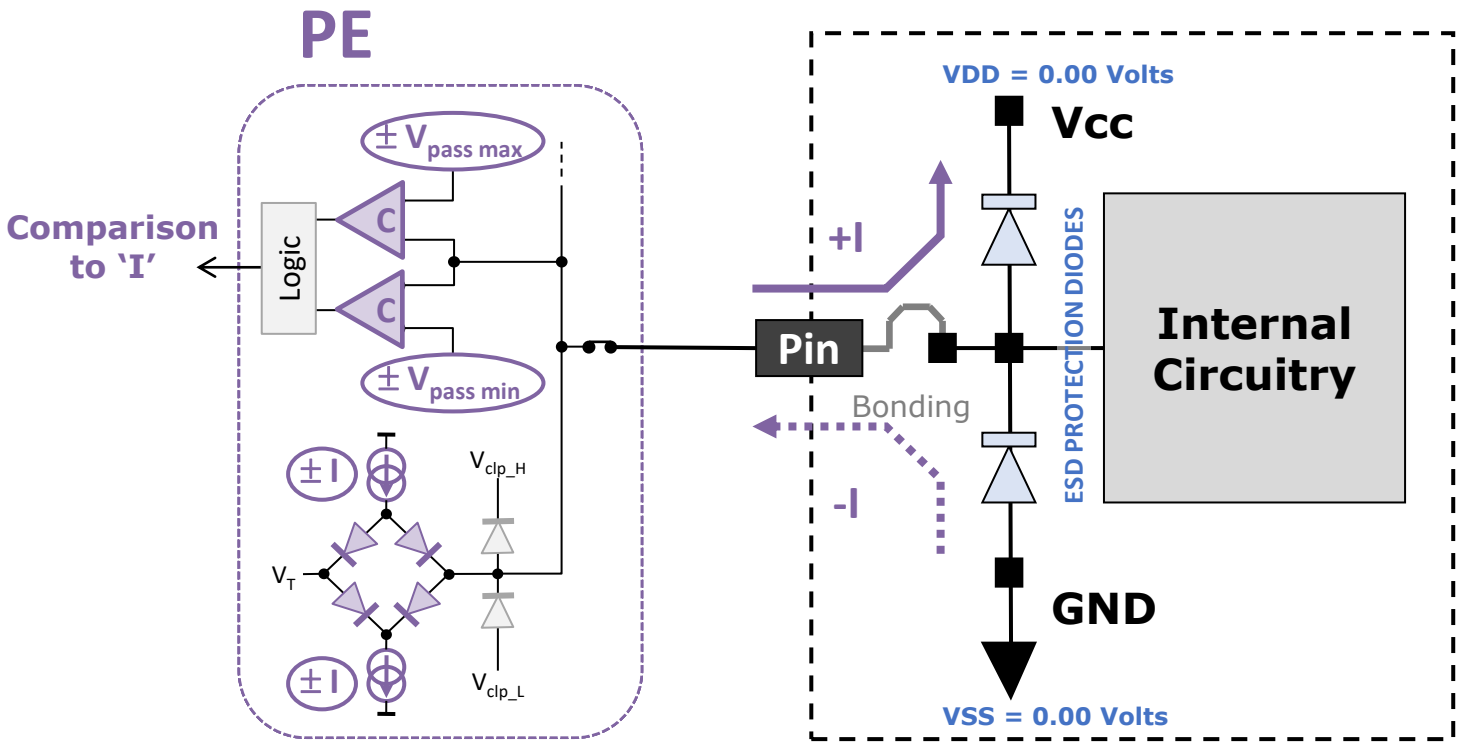
Power supply grounded

3 Test Methods: First Tests

Continuity Test

(also called “Open/Short Test” or “Contact Test”)

- Principle
  - **Force I & Measure V**: resulting voltage should be a <u>diode voltage</u> (ESD protection diodes)



Other option: Implementation with Programmable Load (PL)

⚠ no Meas. Value
Pass/fail result only

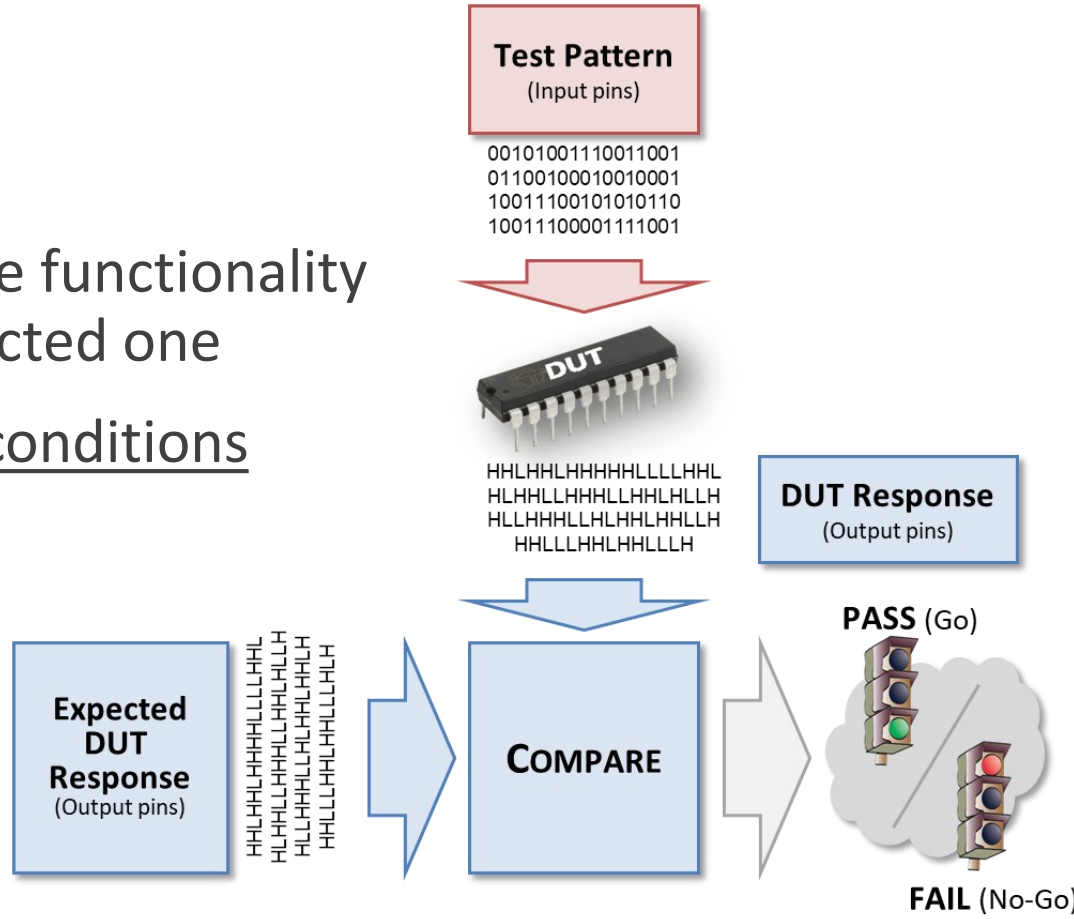
TEST METHODS: FIRST TESTS

FUNCTIONAL TEST

- Purpose
  - Verify that the DUT is functionally “alive”
- Principle
  - Apply a test pattern that exercises the device functionality & compare the DUT response with the expected one
  - Test performed with relaxed level & timing conditions

    - $V_{IL} = 0V,\ \ V_{IH} = V_{CC}$
    - $V_{OL} = \frac{V_{CC}}{2} - 10\% * V_{CC},\ V_{OH} = \frac{V_{CC}}{2} + 10\% * V_{CC}$
    - $f < f_{max}$
    - $T_{setup} > T_{setup-DS},\ \ T_{hold} > T_{hold-DS}$
    - $T_{obs} > T_{prop-DS}$

  - Output: PASS/FAIL result



3 Test Methods: First Tests

Functional vs. Structural Test Approach

Functional

- Test pattern is defined with the objective to **exercise the device functionality**
  - ↳ "manual" generation based on the knowledge of the truth table

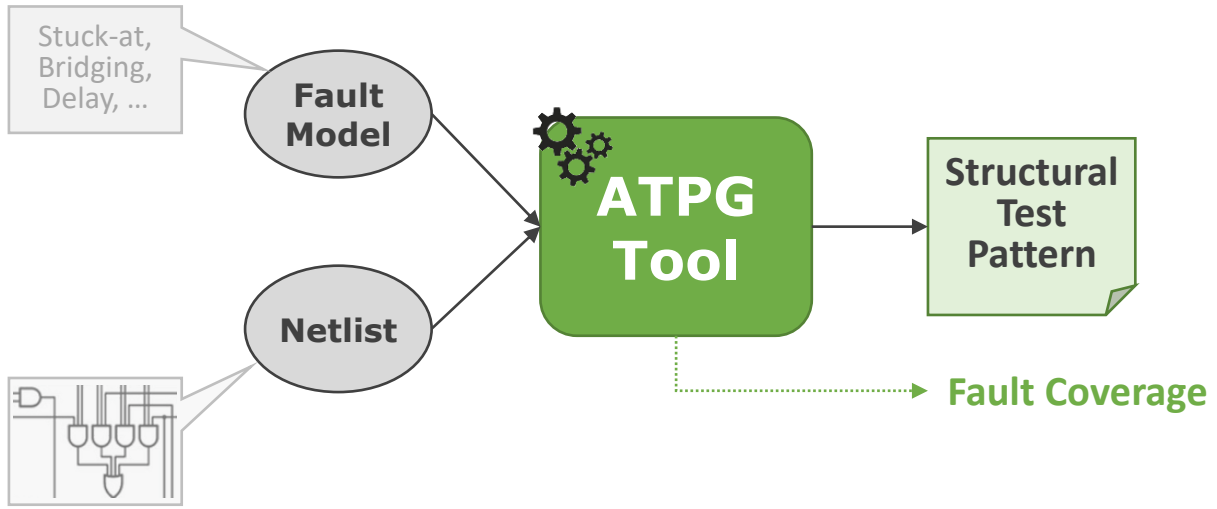
Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

Master reset
Hold
Parallel Load (10000000)
Hold
Shift Right x8 – DS0=0
Parallel Load (01010101)
Shift Left x8 – DS7=1
...

Functional Test Pattern

Structural

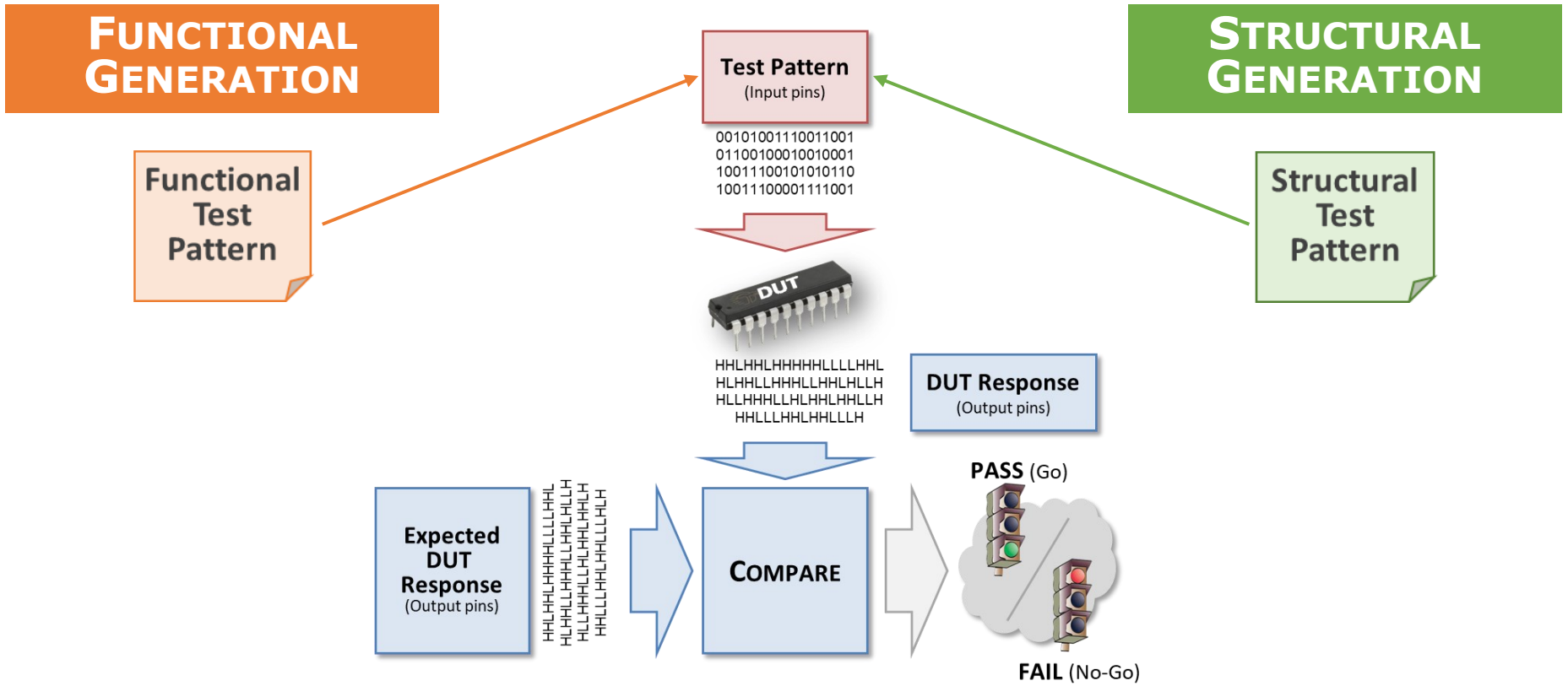
- Test pattern is defined with the objective to **verify the absence of defects**
  - ↳ automatic generation based on fault models & structural circuit description



TEST METHODS: FIRST TESTS

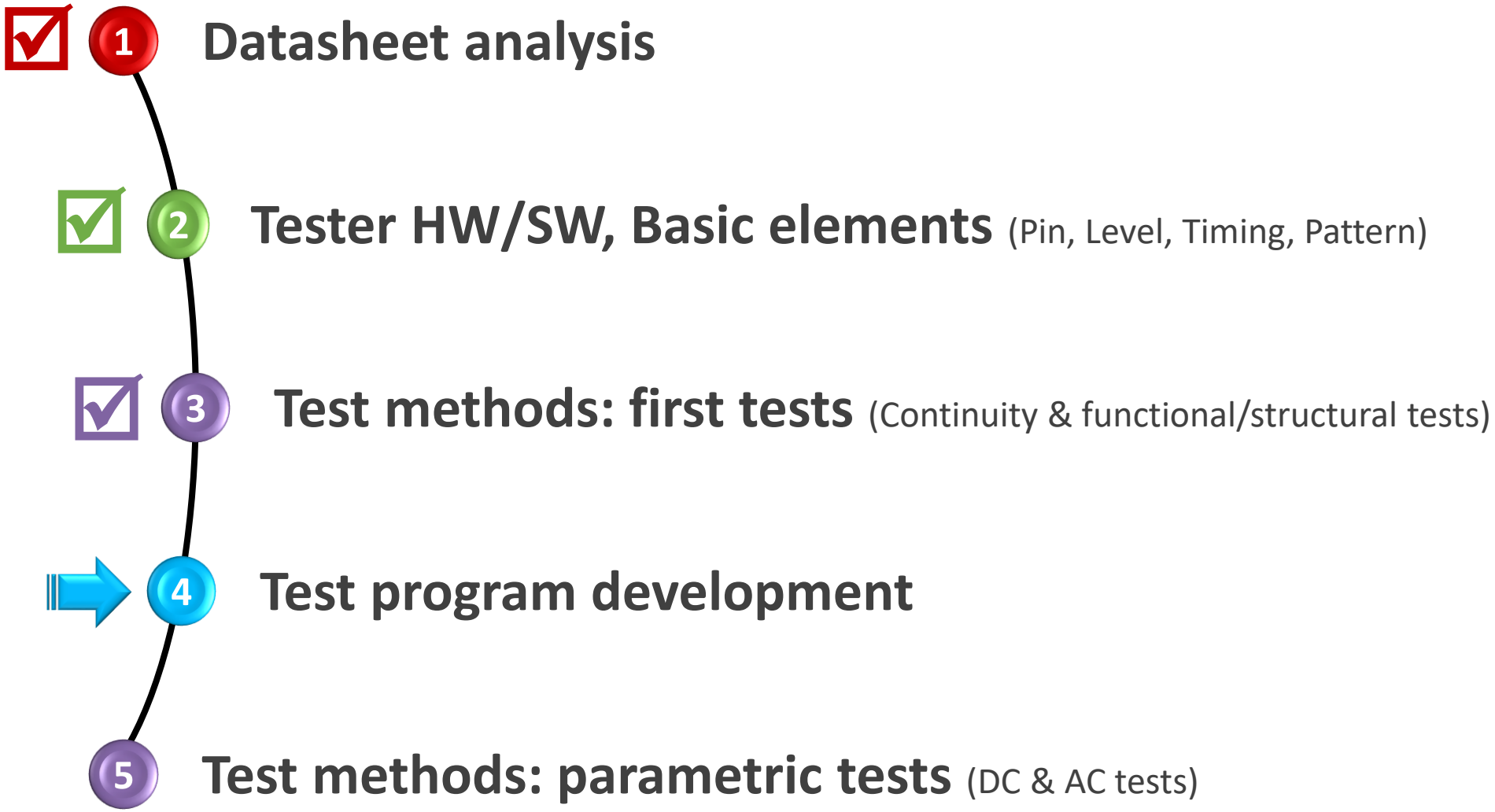
FUNCTIONAL VS. STRUCTURAL TEST APPROACH

- Execution on ATE: no fundamental difference



Exercise:
Questions about First Test Concepts

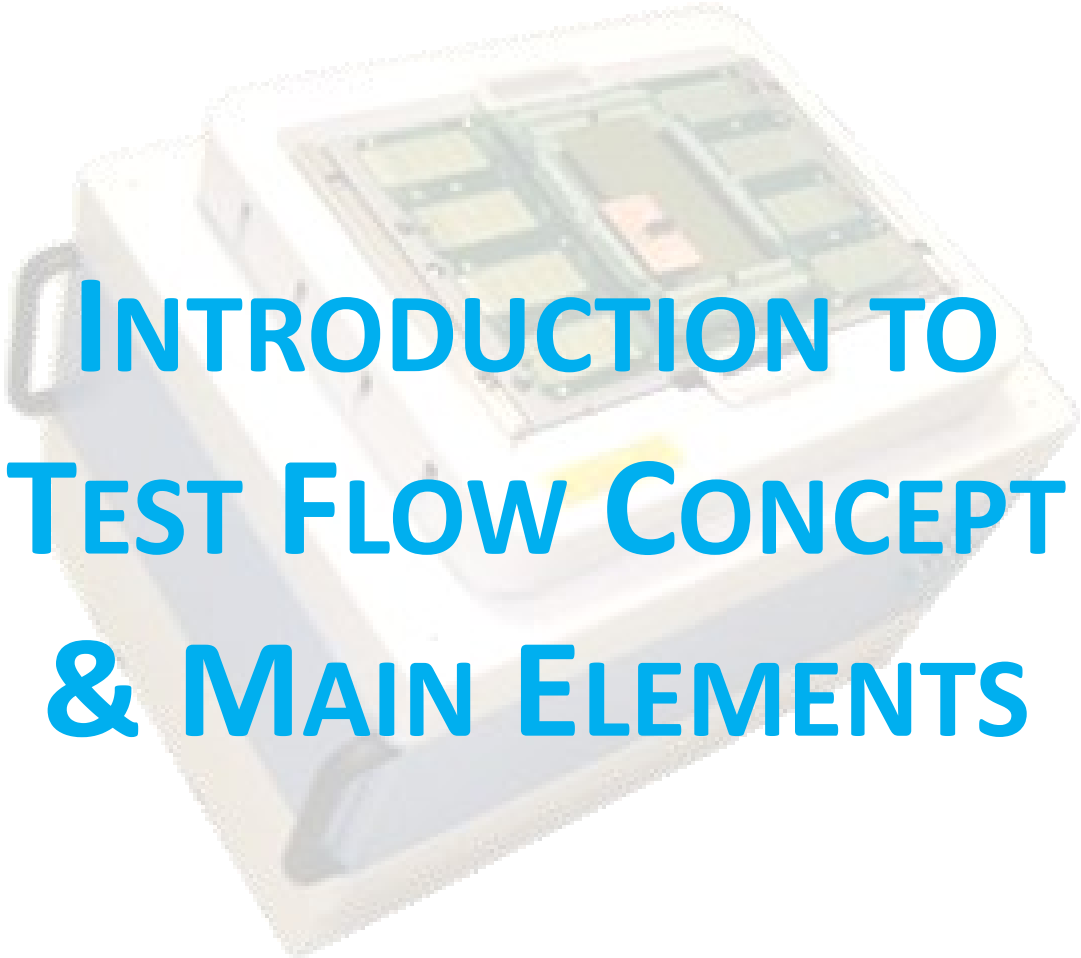
LEARNING STEPS



PART 4

- Test Flow Concept & Main Elements
- Test Flow Creation & Execution in SmarTest

4



Introduction to Test Flow Concept & Main Elements

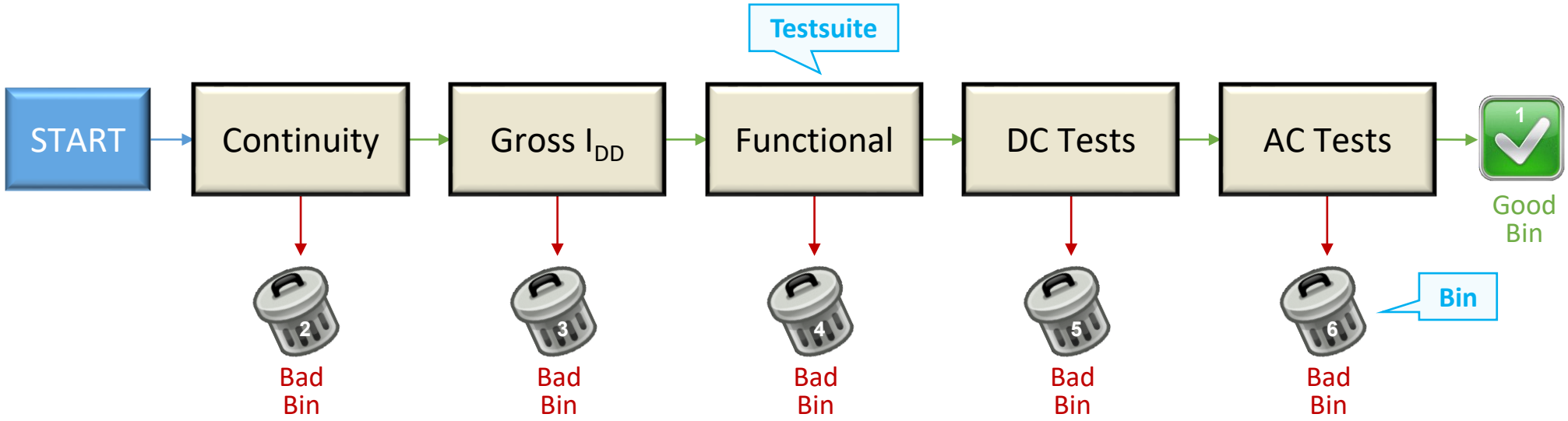
4 TEST FLOW CONCEPT

- Sequential organization of device tests with their bins
- Tests order, pass/fail branching and binning determine the execution of the test flow

Main Test Flow Elements

Testsuites
- Test Method + Level/Timing/Pattern Settings

Bins
- Good or Bad (*STOP point*)



4 TEST FLOW CONCEPT

- Sequential organization of device tests with their bins
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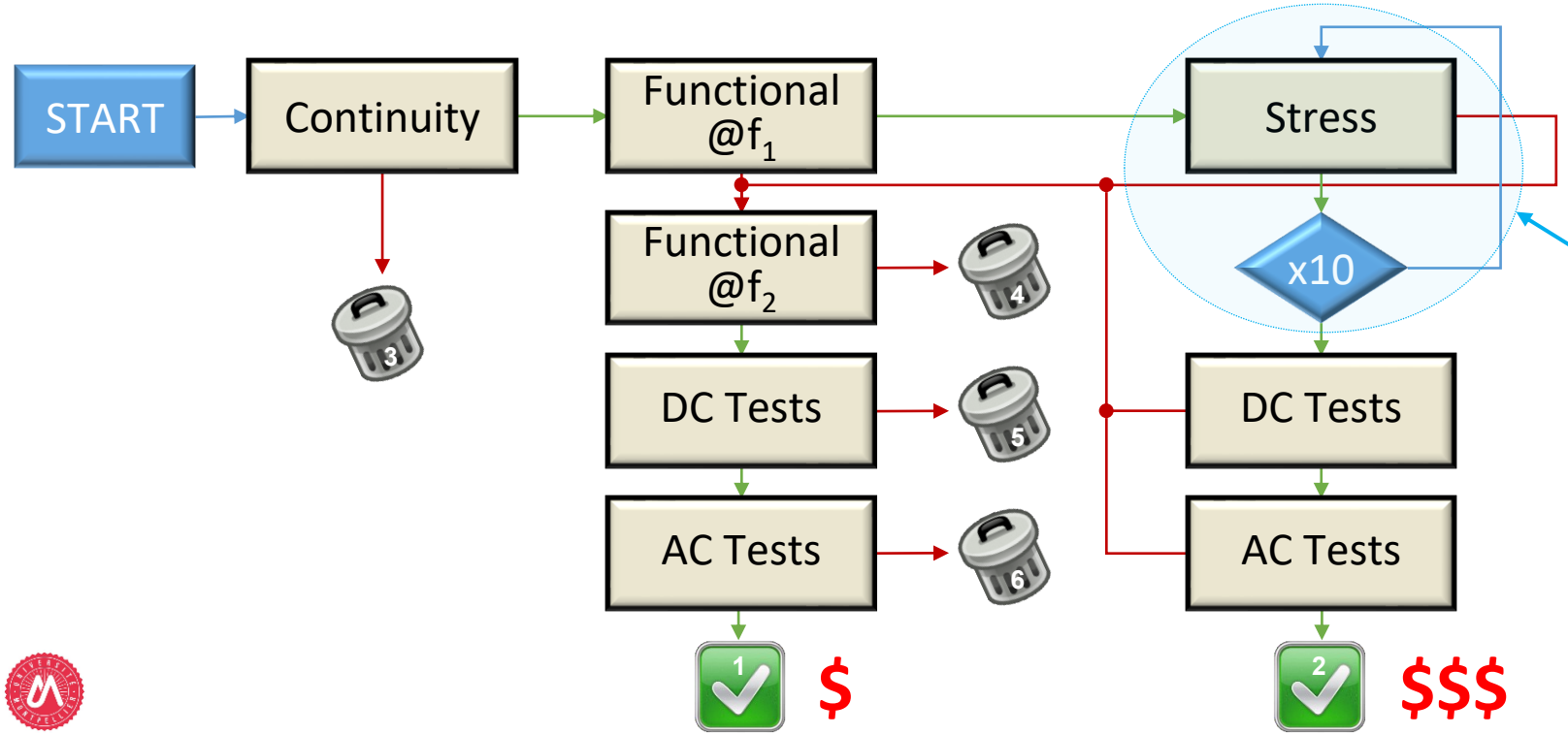


Other Test Flow Elements

Iterative/Conditional Elements

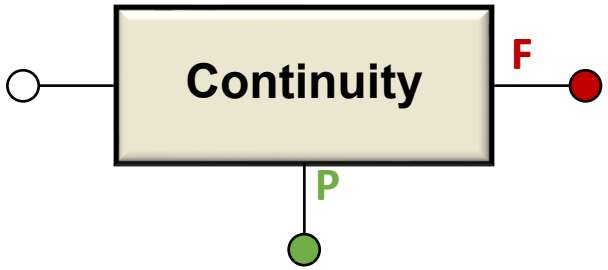
- Repeat Loop
- For Loop
- While Loop
- If/Then

Value Assignments

- Variable
- Level value
- Timing value

4 Test Flow Elements

Testsuite

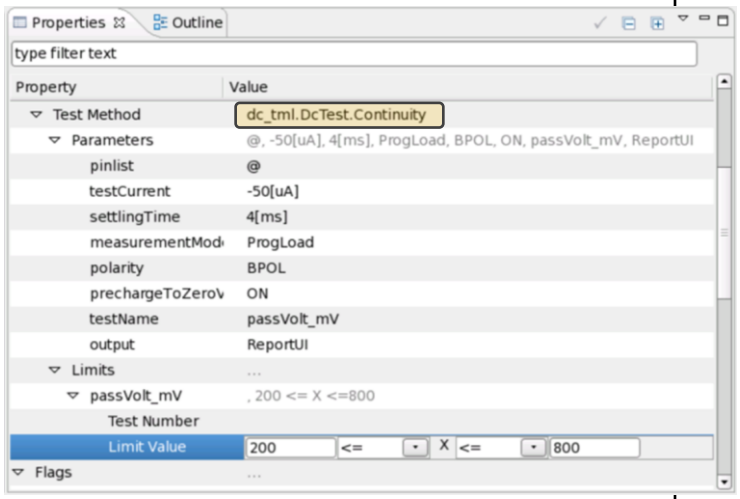


Property	Value
▼ Testsuite	Continuity
▷ Test Method	“DcTest.Continuity”
▼ Primaries	
▷ Timing	1.2.1
▷ Level	2.2.1
▷ Pattern	my_pattern

Test Method

- 2 ways of calling a test method

  - Predefined “Test Function”
    - Only test conditions and limits to fill
    - Hidden firmware code, the user can’t modified
    - Easy to understand for beginners



  - C/C++ code
    - The user programs test conditions, tester HW (relays), test execution, comparison to test limits, test result reporting and P/F outcome
    - Not easy to implement, more flexibility

```
HRESULT Cdigital_tests::continuity(double _results[4])
{
   // add your code
   PPMU_SETTING setting1;
   setting1.pin("@").iForce(50 uA).min(50 mV).max(100 mV).iRange("100uA");

   PPMU_RELAY relay1, relay2;
   relay1.pin("@").status("PPMU_ON");
   relay1.wait(1.3 ms);

   //DISCONNECT PPMU relays
   relay2.pin("@").status("ALL_OFF");
   relay2.wait(1.3 ms);

   PPMU_MEASURE meas1;
   meas1.pin("@").execMode(TM::PVAL);

   TASK_LIST task1;
   task1.add(setting1).add(relay1).add(meas1).add(relay2);
   task1.execute();
   return S_OK;
}
```

Set up: pin to test, force current and limits

Close PPMU relay

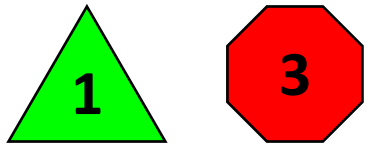
Open PPMU relay

Test technique: value

Task list execution order:
1. Apply setup
2. Close PPMU relay
3. Perform measurements on pins
4. Open PPMU relay

4 TEST FLOW ELEMENTS

GOOD/BAD BIN

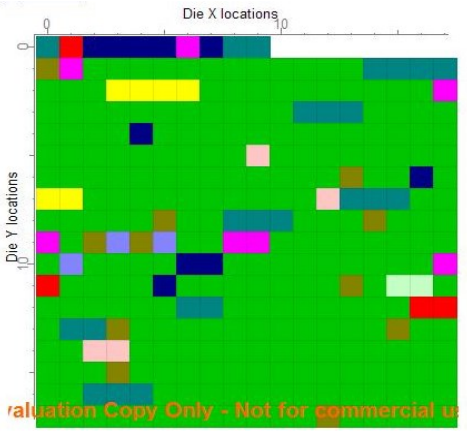


- To sort the devices
- Hardware and software bin numbers defined in the test program
  - Hardware bin number: controls the location where the DUT will be placed (tray or tube) after execution of the test program
  - Software bin number: keeps track of the various pass/fail categories (Statistics)

List of Individual Maps

Top 10 Software Binning	1 PASS	1004 thunderbird_real_bist_max	1400 vil_vih_vol_voh_max	1630 idd sleep max	601 thunderbird_ct_max	600 thunderbird_ic_max	1110 cont_pwr	500 thunderbird_ic_min	700 lvdsTest070731_nom	Others
Color										-
Pass/Fail	P	F	F	F	F	F	F	F	F	-
Percentage	77.8%	7.3%	3.5%	3.2%	2.2%	1.9%	1.3%	1.3%	0.9%	0.6%
Total count	246	23	11	10	7	6	4	4	3	2

File	D:/Qualtera/Galaxy/P61222.0U_9D00646101_20071228103119.stdf
Map style	STRIP map (parts tested are PACKAGED DEVICES!)
Total physical parts tested	316
Parts processed	All Data / parts (any Bin)
Data from Sites	All sites
Product	om6361
Lot	P61222.0U
SubLot	9D00646101
Strip ID:	P61222.0U-9D00646101
Strip started	ven. déc. 28 13:54:09 2007
Map dimensions	LowX=0, LowY=0, HighX=17, HighY=17



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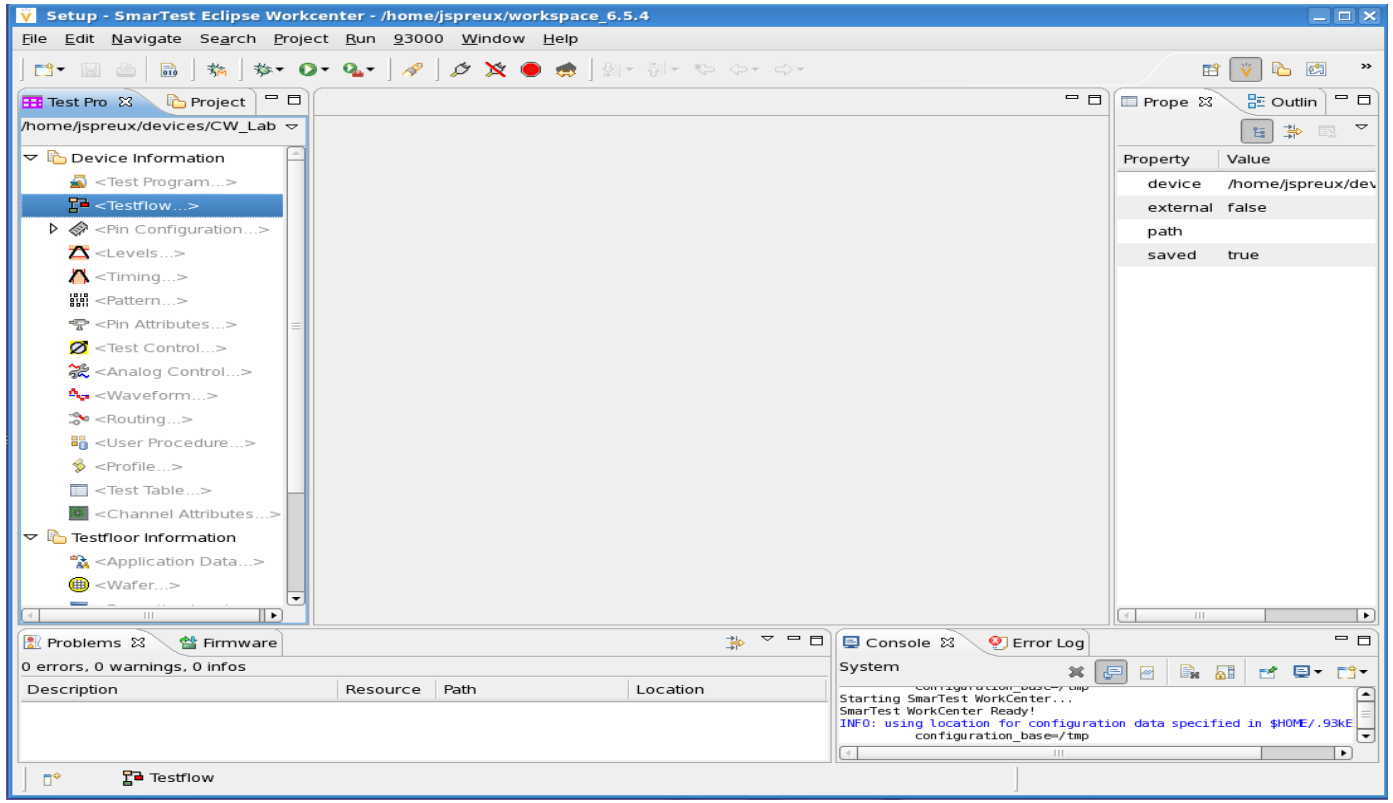
TEST FLOW CREATION & EXECUTION IN SMARTEST

TEST FLOW CREATION & EXECUTION

TEST FLOW CREATION IN SMARTEST

MAIN STEPS

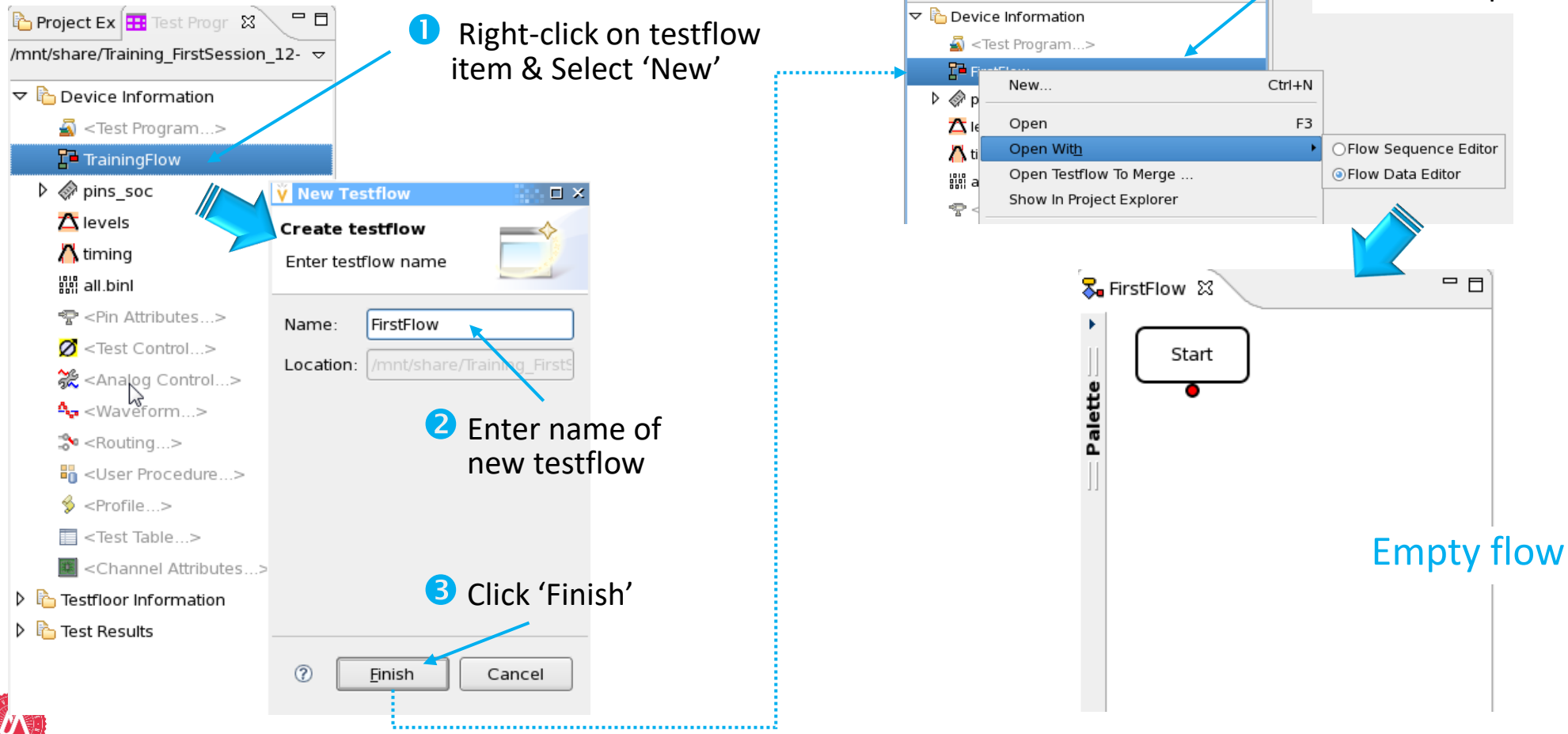
1. **Create new testflow**
2. **Setup the "context"**
3. **Insert elements**
   (Testsuites & Bins)
4. **Save testflow**



4 TEST FLOW CREATION & EXECUTION

1. Create new testflow

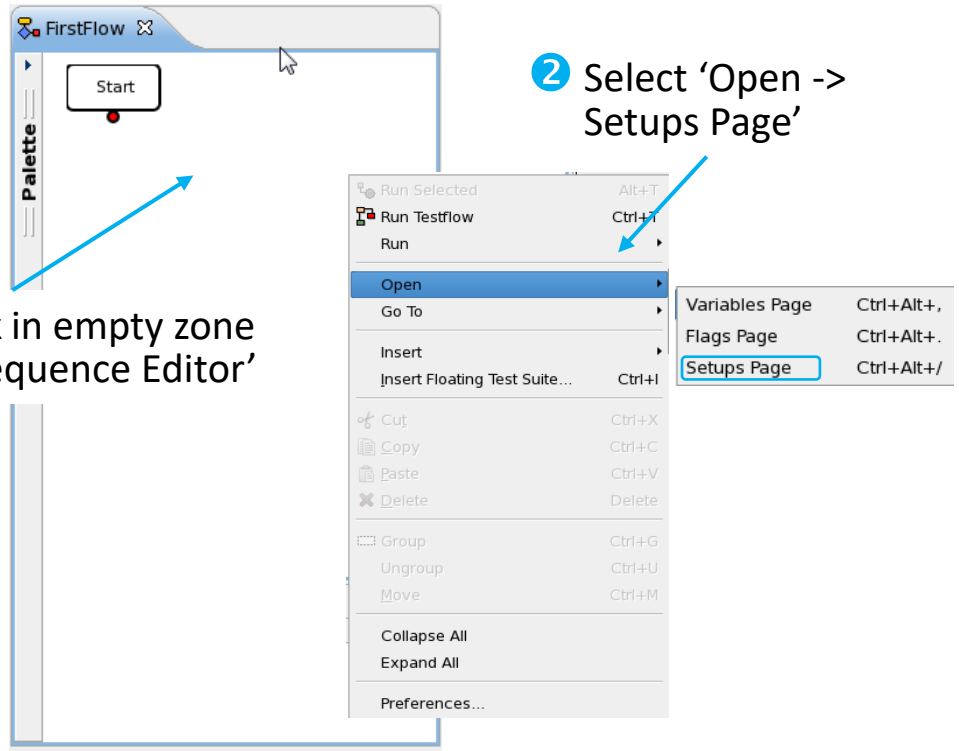
TEST FLOW CREATION IN SMARTEST



4 TEST FLOW CREATION & EXECUTION

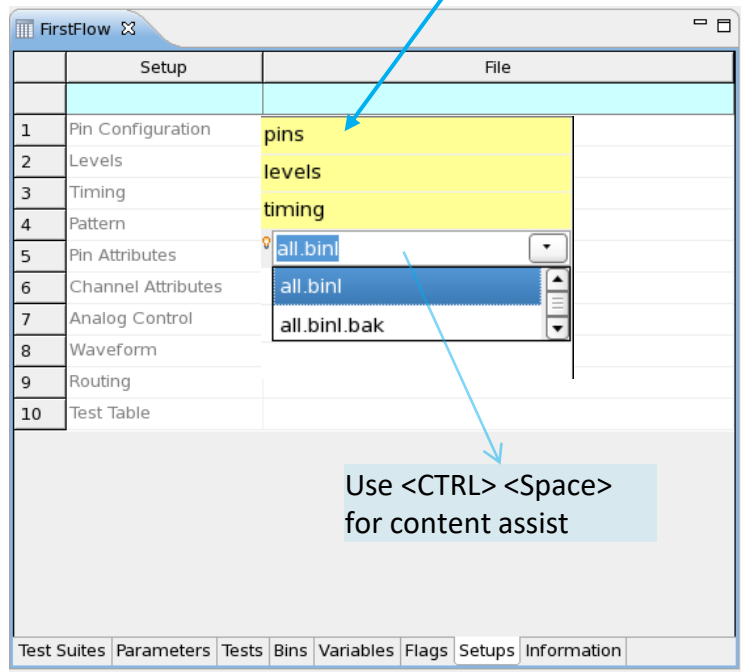
2. Setup files assignation

TEST FLOW CREATION IN SMARTEST



❶ Right-click in empty zone of 'Flow Sequence Editor'

❷ Select 'Open -> Setups Page'



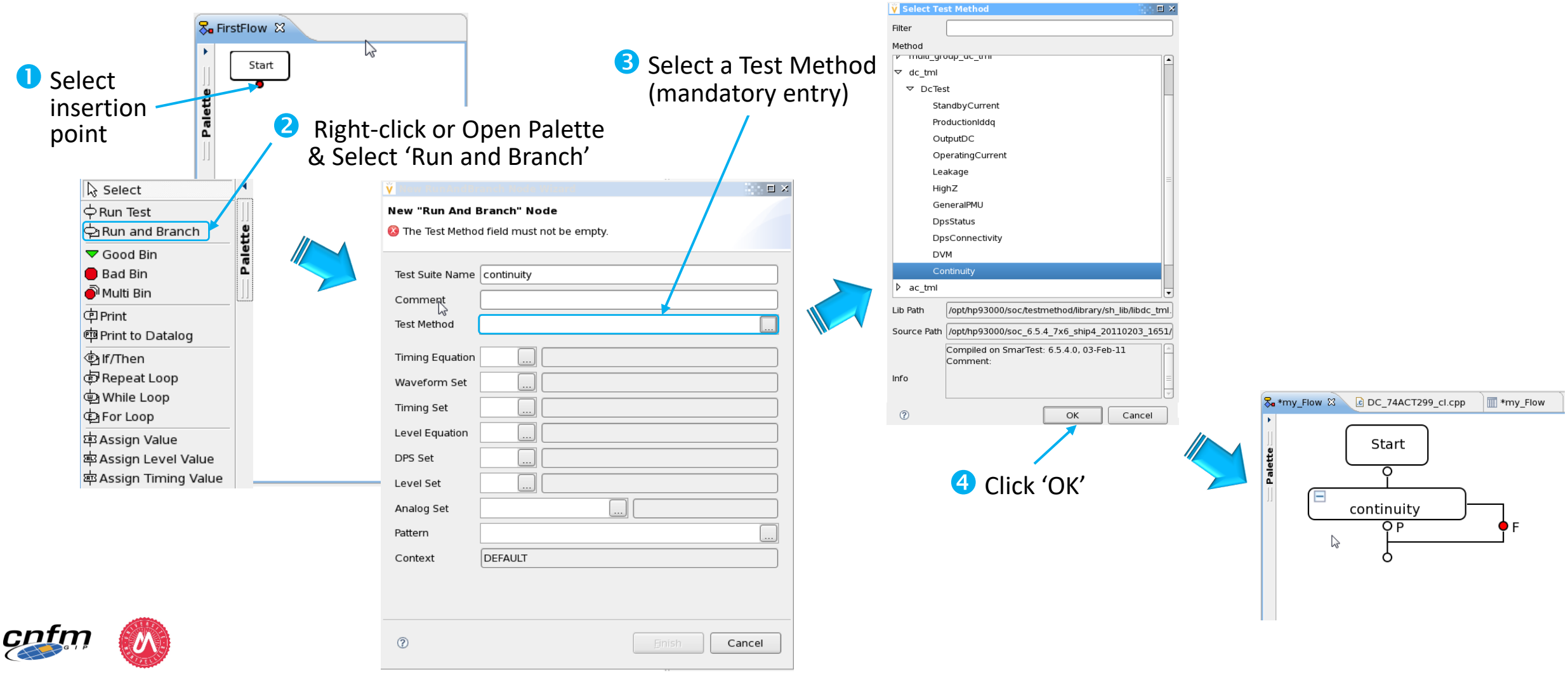
❸ Fill in your primary setup files

Necessary step to make all primary settings (pins/level/timing/pattern) available within the Testflow

4 TEST FLOW CREATION & EXECUTION

3. Element insertion
Testsuite

TEST FLOW CREATION IN SMARTEST

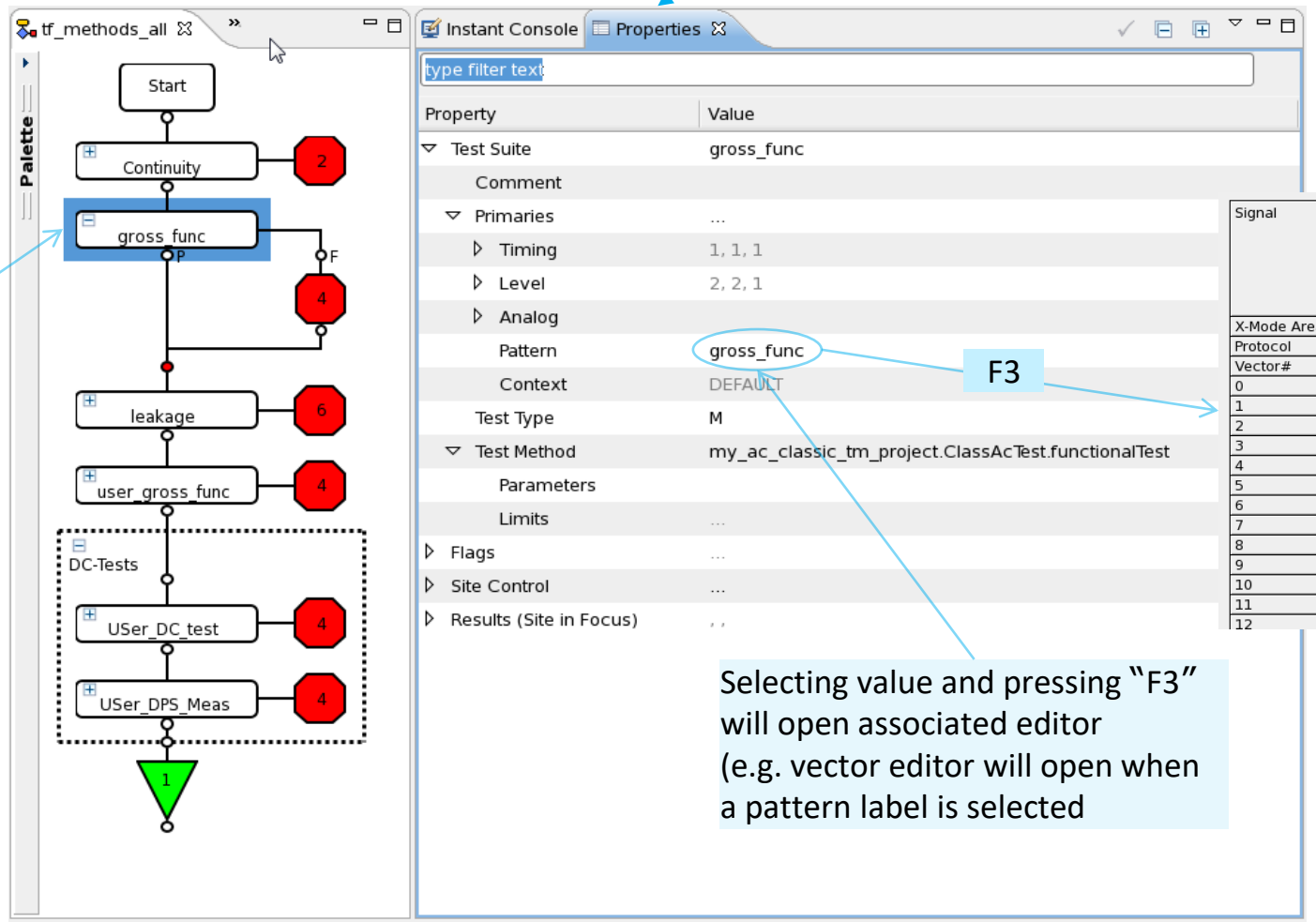


3. Element insertion
Testsuite

TEST FLOW CREATION IN SMARTEST

PROPERTIES VIEW

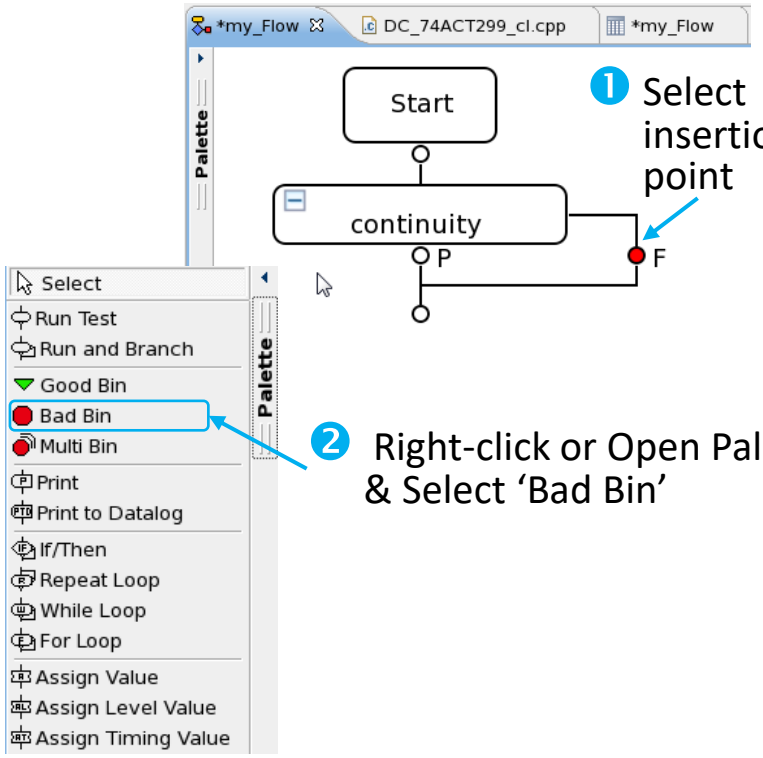
Double-click on Testsuite will open the Properties view



Selecting value and pressing "F3" will open associated editor (e.g. vector editor will open when a pattern label is selected

3. Element insertion
Bin

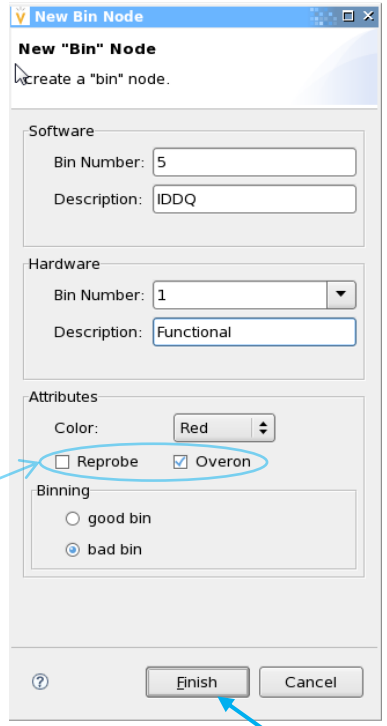
TEST FLOW CREATION IN SMARTEST

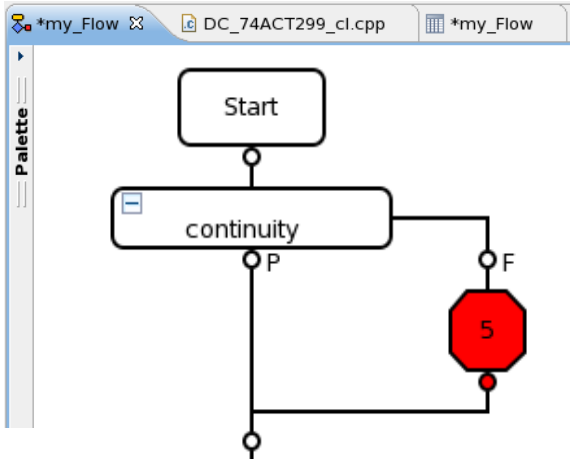


❶ Select insertion point

❷ Right-click or Open Palette & Select 'Bad Bin'

❸ Fill the entries





Attributes
- Reprobe: used for wafer-level testing
- Overon: used for debug during test flow development

❹ Click 'Finish'

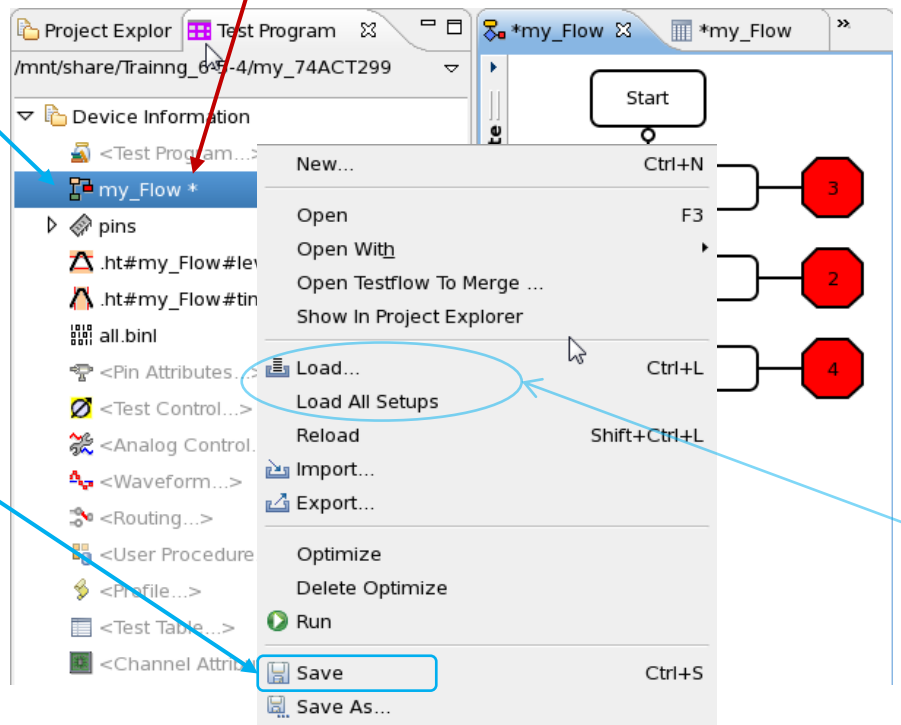
4. Save testflow

TEST FLOW CREATION IN SMARTEST

*: changes done in testflow ➔ Save REQUIRED

❶ Right-click on testflow item in Test Program Explorer

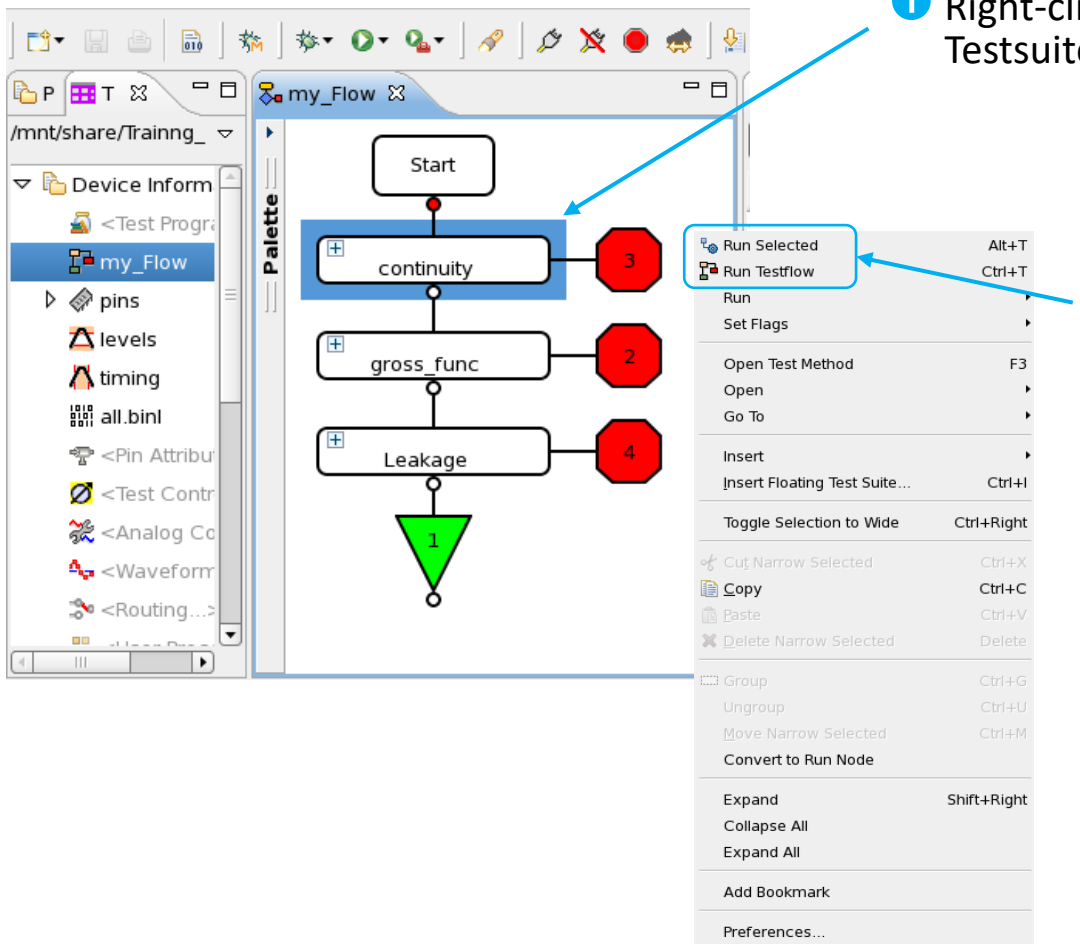
❷ Select 'Save'



Loading Process in two steps
- 'Load': will open 'Select file to load'
- 'Load All Setups': will fill tester-hardware with primary data

TEST FLOW CREATION & EXECUTION

TEST FLOW EXECUTION IN SMARTEST



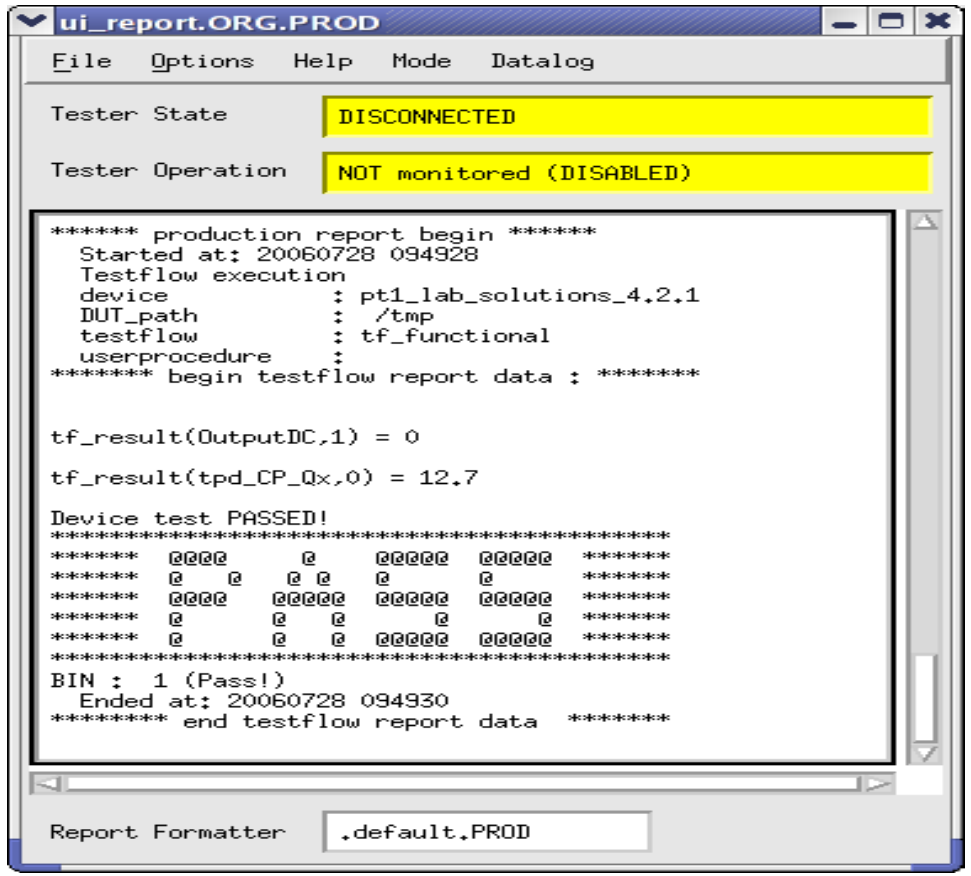
❶ Right-click on a Testsuite

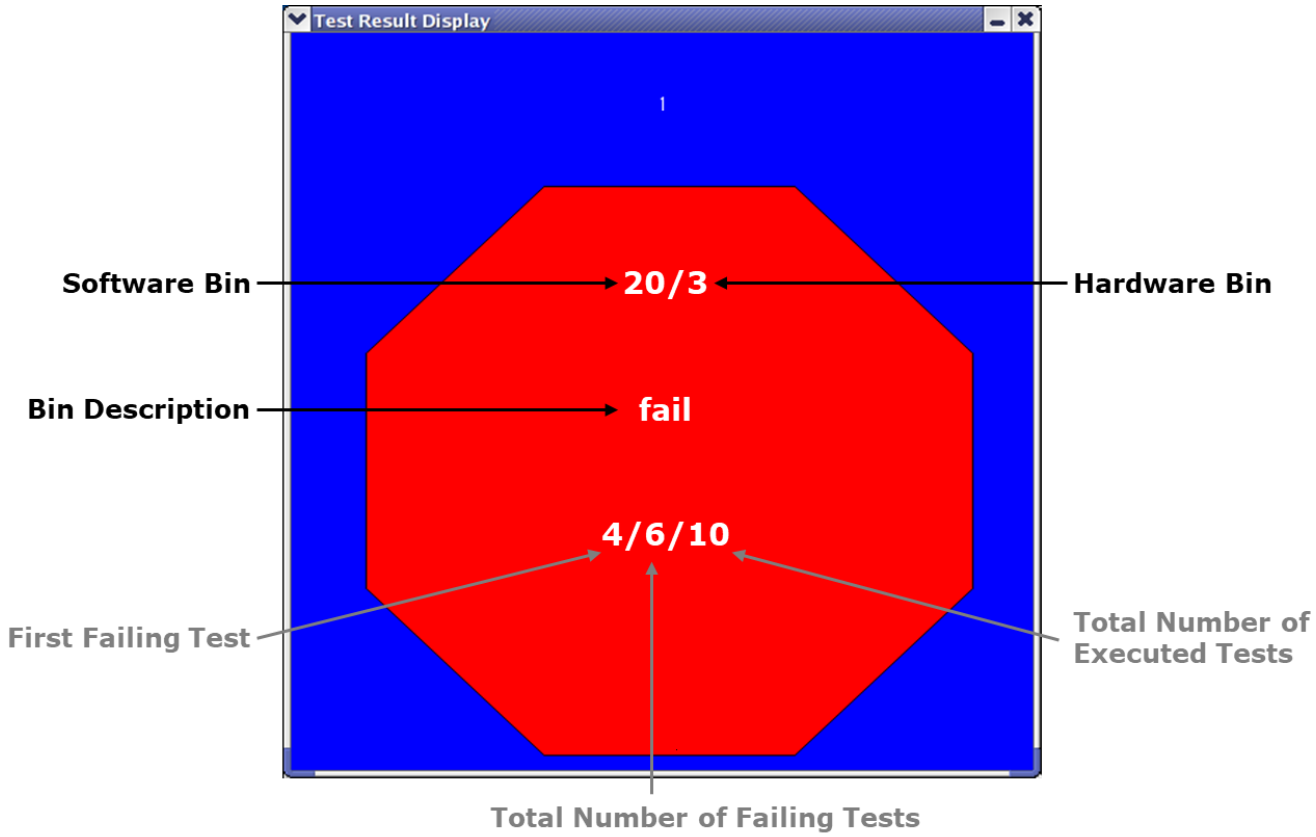
❷ Choose

- 'Run Selected': single Testsuite execution
- 'Run Testflow': overall Testflow execution

4 TEST FLOW CREATION & EXECUTION

TEST FLOW EXECUTION IN SMARTEST



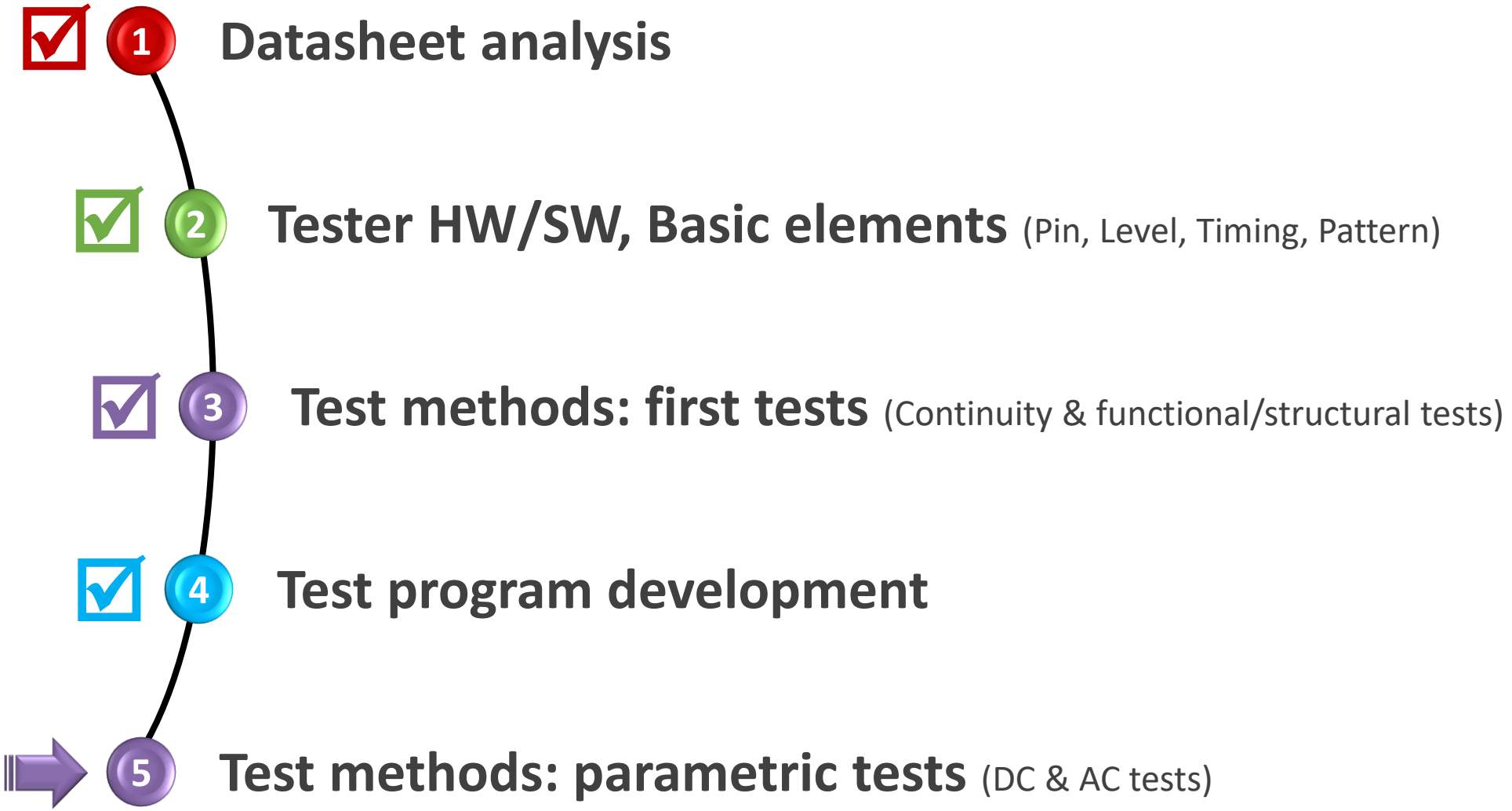


4

Lab & Exercises:

74ACT299 Test Program Development:
First Test Flow *(off-line + on-line)*

LEARNING STEPS



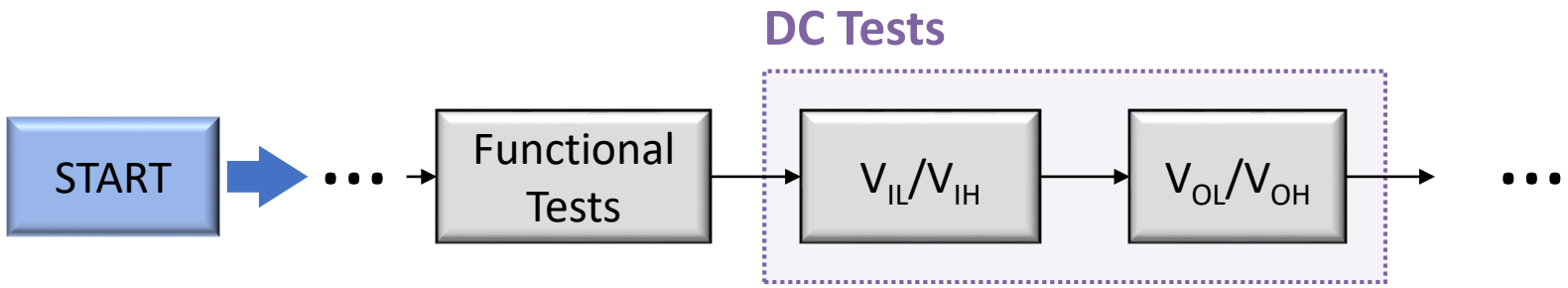
3 TEST METHODS: PARAMETRIC TESTS

- Production Test Flow

Test Methods: DC Parametric Tests

DC Tests

- Purpose
  - Verify device DC performances, once functionality is OK
- Classical Tests
  - V_{IL}/V_{IH}, V_{OL}/V_{OH}

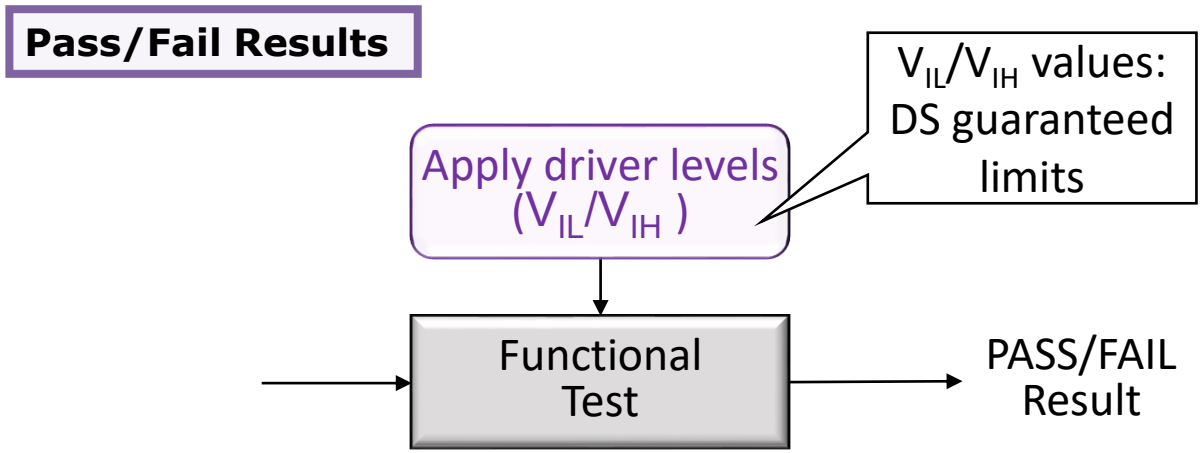


Can be based on functional tests or on V/I measurements

5 Test Methods: DC Parametric Tests

V_{IL}/V_{IH} Test

- Purpose
  - Ensure that the input pins can correctly sense the proper logic levels when programmed V_{IL}/V_{IH} voltages are applied
- Principle
  - Functional test with driver levels configured at datasheet V_{IL}/V_{IH} values for input pins *(relaxed constraints on comparator levels for output pins)*



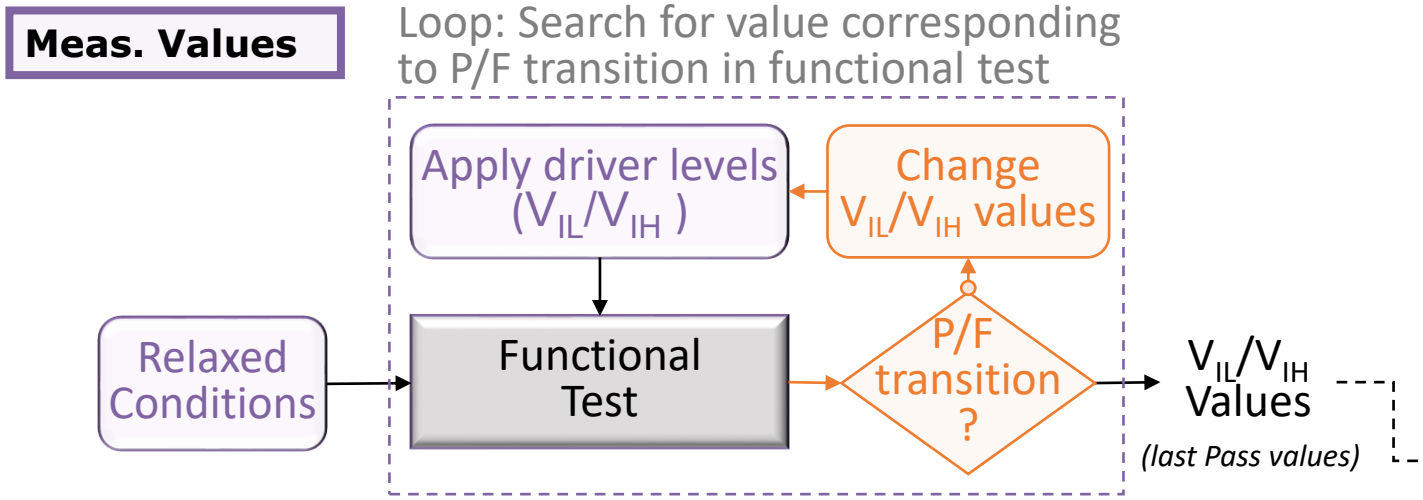
DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
		4.5	1.5	0.8	0.8		

5 TEST METHODS: DC PARAMETRIC TESTS

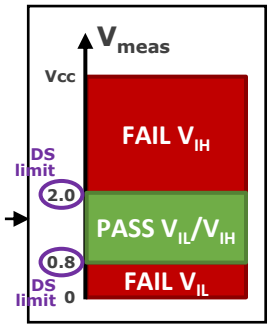
V_{IL}/V_{IH} TEST

- Purpose
  - Ensure that the input pins can correctly sense the proper logic levels when programmed V_{IL}/V_{IH} voltages are applied
- Principle
  - Iterations of functional test with changing of V_{IL}/V_{IH} values for input pins *(relaxed constraints on comparator levels for output pins)*



DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = –40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
		4.5	1.5	0.8	0.8		



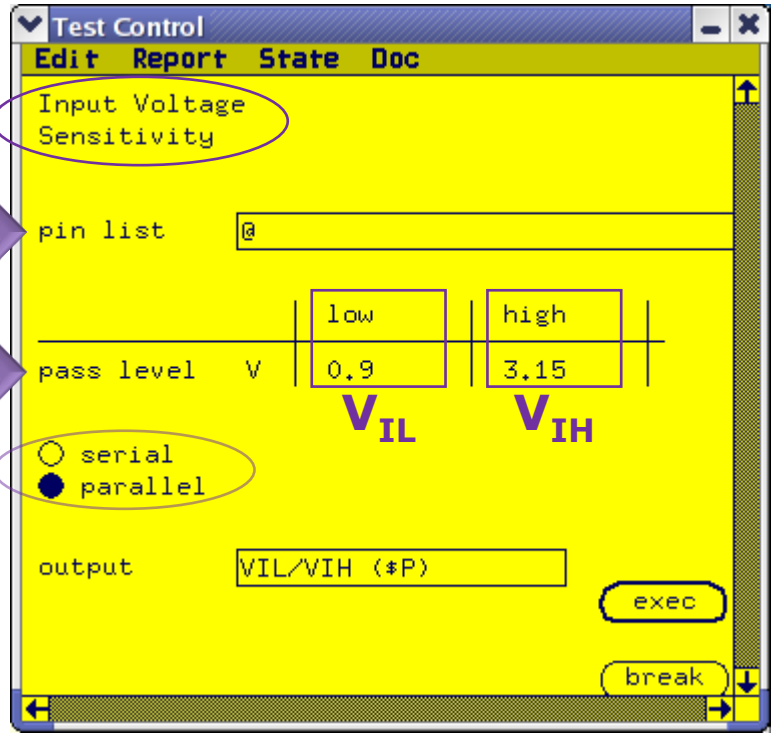
V_{IL}/V_{IH} Test Result

- PASS if $V_{IL\text{-meas}} \geq V_{IL\text{-limit}}$ & $V_{IH\text{-meas}} \leq V_{IH\_limit}$
- FAIL otherwise

5 Test Methods: DC Parametric Tests

V_{IL}/V_{IH} Test in SmarTest

Test Function: 'Input Voltage Sensitivity'



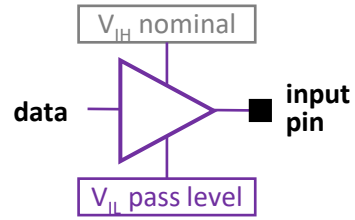
Pin list

Pass Limits

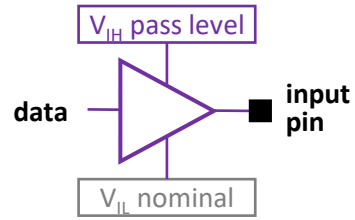
- 'Serial': Result for each pin
- 'Parallel': Global result for the pin list

Test Procedure

1. Set V_{IL} to low pass level
   Execute functional test



2. Set V_{IH} to high pass level
   Set back V_{IL} to nominal level
   Execute functional test



3. Return FAIL if either execution fails, otherwise return PASS

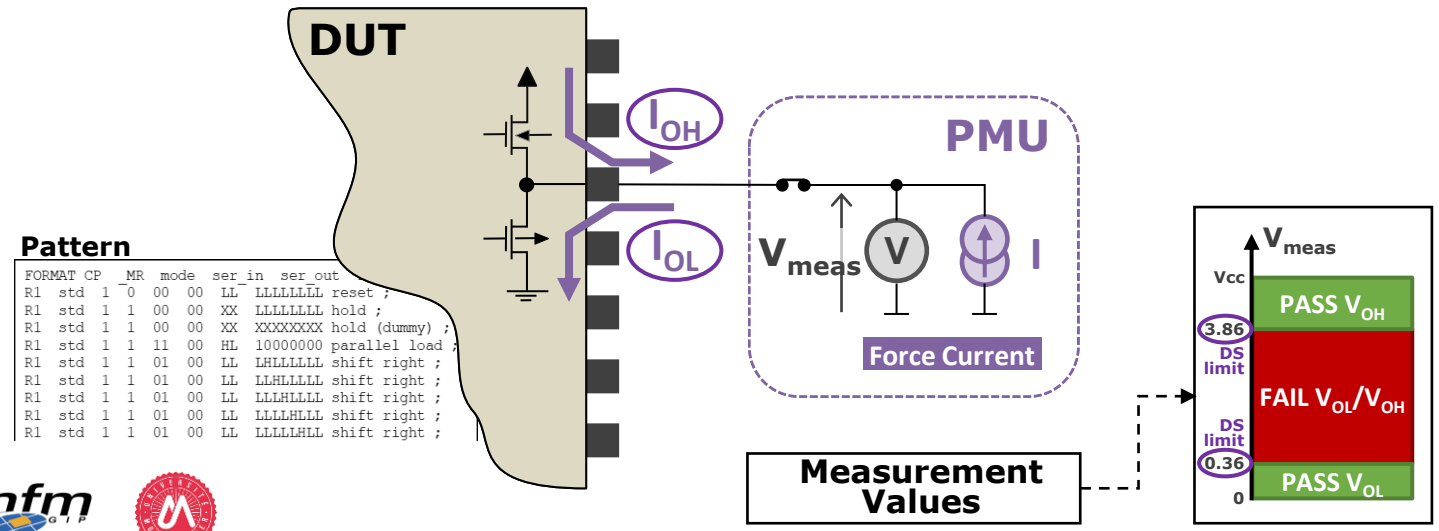
* *V_{IL}/V_{IH} measurement: iterations of steps 1 & 2 with incremental change of V_{IL}/V_{IH} setting to identify P/F transition (meas. value = last Pass value) Return FAIL if measured V_{IL} < low pass level or measured V_{IH} > high pass level, otherwise return PASS*

5 Test Methods: DC Parametric Tests

V_{OL}/V_{OH} Test

- Purpose
  - Verify voltage/current capabilities: ensure that the V_{OL}/V_{OH} voltages are not too much degraded while output pins deliver the specified I_{OL}/I_{OH} current
- Principle
  - Force I_{OL}/I_{OH} current on output pins and measure the corresponding V_{OL}/V_{OH} voltage

Implementation with PMU



DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{OH}	Minimum HIGH Level	4.5	4.49	4.4	V	I_{OUT} = −50 µA
		5.5	5.49	5.4		
		4.5	0.0001	3.86	V	V_{IN} = V_{IL} or V_{IH}
		5.5		4.86		I_{OH} = −24 mA
				3.76		I_{OH} = −24 mA (Note 5)
				4.76		
V_{OL}	Maximum LOW Level	4.5	0.001	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.001	0.1		
		4.5		0.36	V	V_{IN} = V_{IL} or V_{IH}
		5.5		0.36		I_{OL} = 24 mA
				0.44		I_{OL} = 24 mA (Note 5)
				0.44		

V_{OL}/V_{OH} Test Result

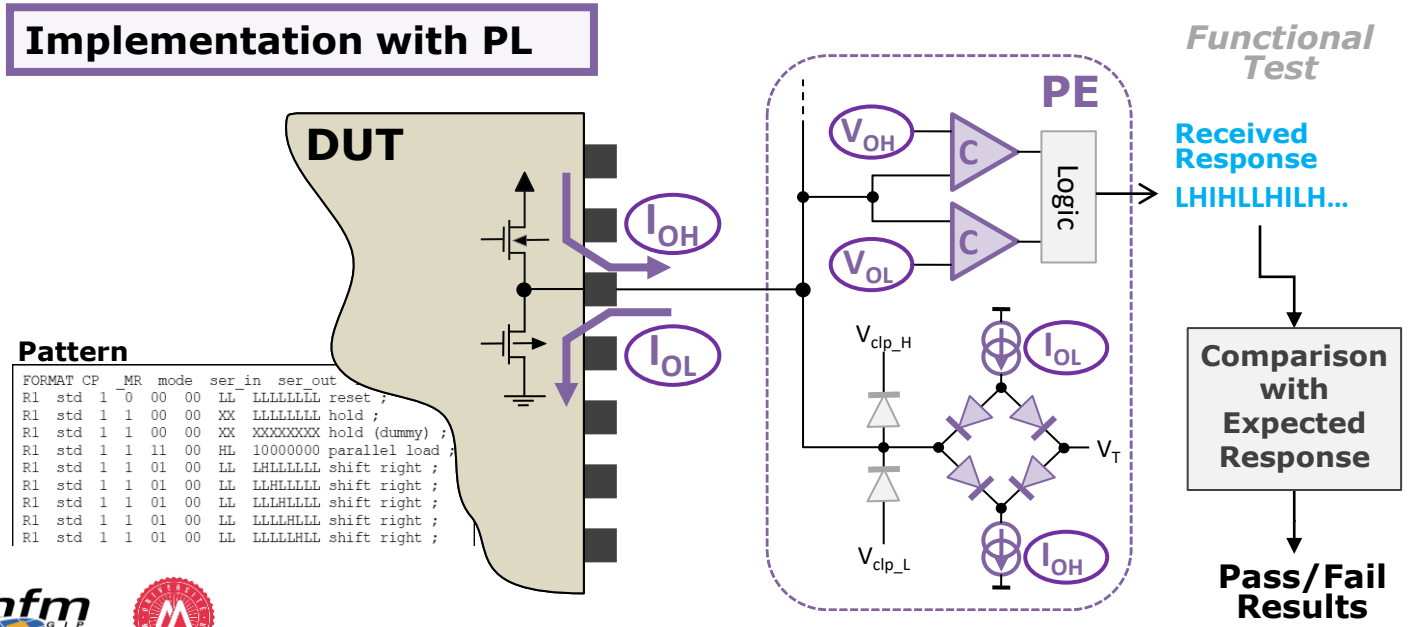
- PASS if $V_{OL\text{-}meas} \leq V_{OL\text{-}limit}$ & $V_{OH\text{-}meas} \geq V_{OH\_limit}$
- FAIL otherwise

5 TEST METHODS: DC PARAMETRIC TESTS

V_{OL}/V_{OH} TEST

- Purpose
  - Verify voltage/current capabilities: ensure that the V_{OL}/V_{OH} voltages are not too much degraded while output pins deliver the specified I_{OL}/I_{OH} current
- Principle
  - Force I_{OL}/I_{OH} current on output pins and measure the corresponding V_{OL}/V_{OH} voltage

Implementation with PL



Pattern

```
FORMAT CP   _MR  mode  ser_in  ser_out
R1  std  1  0   00   00   LL   LLLLLLL reset ;
R1  std  1  1   00   00   XX   LLLLLLL hold ;
R1  std  1  1   00   00   XX   XXXXXXX hold (dummy) ;
R1  std  1  1   11   00   HL   10000000 parallel load ;
R1  std  1  1   01   00   LL   LHLLLLL shift right ;
R1  std  1  1   01   00   LL   LLHLLLL shift right ;
R1  std  1  1   01   00   LL   LLLHLLL shift right ;
R1  std  1  1   01   00   LL   LLLLHLL shift right ;
R1  std  1  1   01   00   LL   LLLLLHL shift right ;
```

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{OH}	Minimum HIGH Level	4.5	4.49	4.4	V	I_{OUT} = −50 µA
		5.5	5.49	5.4		
		4.5	0.0001	3.86	V	V_{IN} = V_{IL} or V_{IH}
		5.5		4.86		I_{OH} = −24 mA (Note 5)
		4.5		3.76		I_{OH} = −24 mA
		5.5		4.76		
V_{OL}	Maximum LOW Level	4.5	0.001	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.001	0.1		
		4.5		0.36	V	V_{IN} = V_{IL} or V_{IH}
		5.5		0.36		I_{OL}= 24 mA (Note 5)
		4.5		0.44		I_{OL}= 24 mA
		5.5		0.44		

If measurement values are demanded:

- *Iterations of functional test to identify P/F transition (meas. values = last Pass values)*
- *Comparison of meas. values with V_{OL}/V_{OH} limits to return a Pass/Fail result*

TEST METHODS: DC PARAMETRIC TESTS

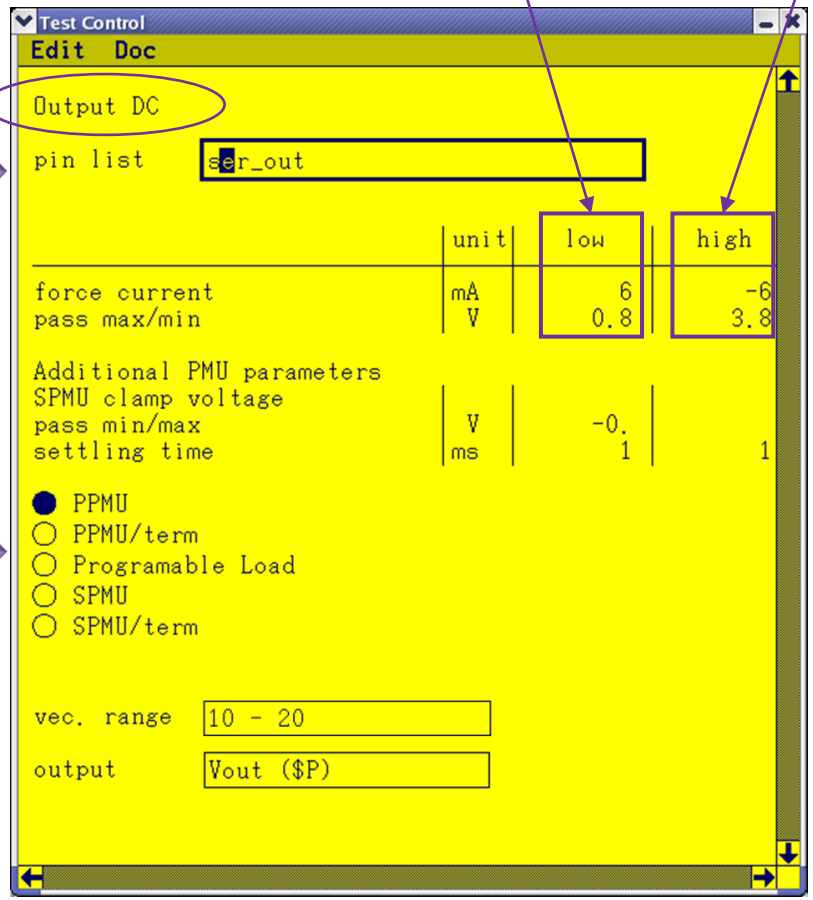
V_{OL}/V_{OH} TEST IN SMARTEST

Test Function: 'Output DC'

I_{OL}/V_{OL} I_{OH}/V_{OH}

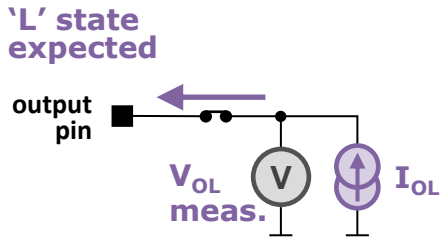
Pin list

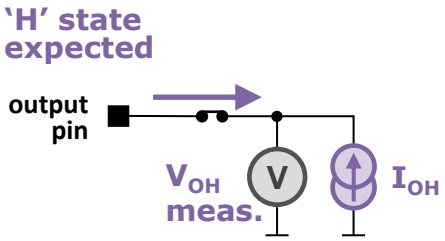
Instrument



Test Procedure with PMU option

1. Execute test vectors; Scan for 'L' or 'H' state in a pin-by-pin basis
2. For first pin & for each vector: Connect PMU, Force Current@spec value & Measure Voltage





3. Repeat for remaining pins
4. Compare to pass values

5 Test Methods: DC Parametric Tests

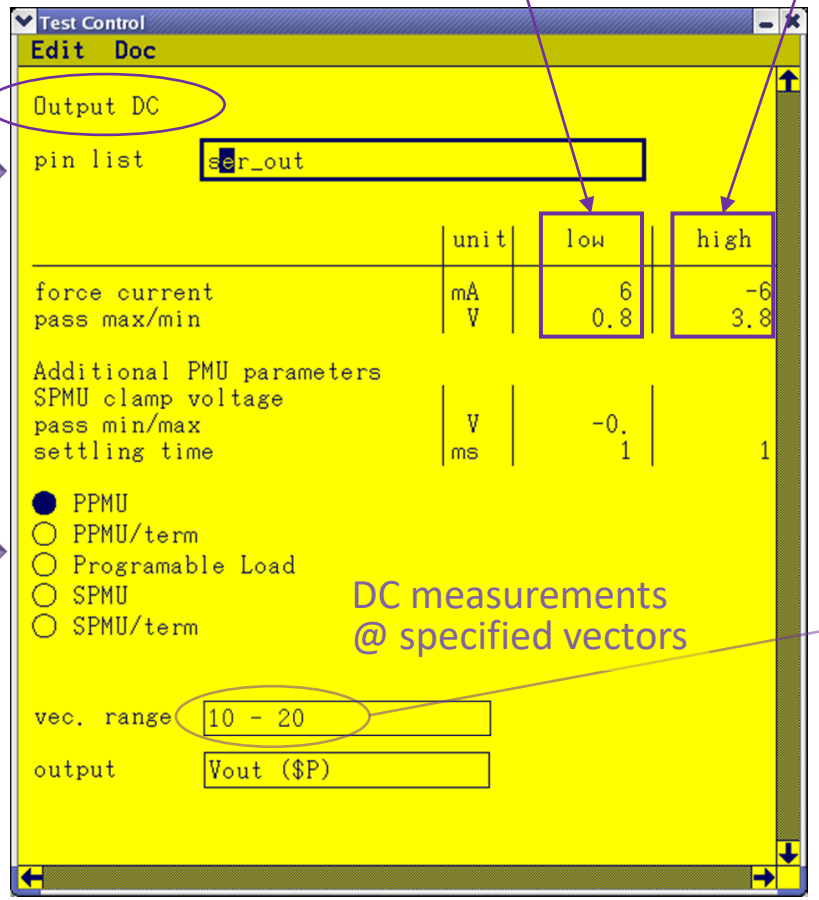
V_{OL}/V_{OH} Test in SmarTest

Test Function: 'Output DC'

I_{OL}/V_{OL} I_{OH}/V_{OH}

Pin list

Instrument



Test Procedure with PMU option

1. Execute test vectors; Scan for 'L' or 'H' state in a pin-by-pin basis in the specified vector range

Make sure that both 'L' & 'H' states are present in the specified vector range for the pins under test

```
FORMAT CP   _MR  mode  ser_in  ser_out  io_pins ;
R1   std  1   0   00   00   LL   LLLLLLLL reset ;
R1   std  1   1   00   00   XX   LLLLLLLL hold ;
R1   std  1   1   00   00   XX   XXXXXXXX hold (dummy) ;
R1   std  1   1   11   00   HL   10000000 parallel load ;
R1   std  1   1   01   00   LL   LHLLLLLL shift right ;
R1   std  1   1   01   00   LL   LLHLLLLL shift right ;
R1   std  1   1   01   00   LL   LLLHLLLL shift right ;
R1   std  1   1   01   00   LL   LLLLHLLL shift right ;
R1   std  1   1   01   00   LL   LLLLLHLL shift right ;
R1   std  1   1   01   00   LL   LLLLLLHL shift right ;
R1   std  1   1   01   00   LH   LLLLLLLH shift right ;
R1   std  1   1   01   00   LL   LLLLLLLL shift right ;
R1   std  1   1   10   01   LH   LLLLLLLH shift in left ;
R1   std  1   1   10   01   LH   LLLLLLHH shift in left ;
R1   std  1   1   10   00   LL   LLLLLHHL shift left ;
R1   std  1   1   10   00   LL   LLLLHHLL shift left ;
R1   std  1   1   10   00   LL   LLLHHLLL shift left ;
R1   std  1   1   10   00   LL   LLHHLLLL shift left ;
R1   std  1   1   10   00   LL   LHHLLLLL shift left ;
R1   std  1   1   10   00   HL   HHLLLLLL shift left ;
R1   std  1   1   10   00   HL   HLLLLLLL shift left ;
R10  std  1   1   00   00   XX   HLLLLLLL hold ;
```

TEST METHODS: DC PARAMETRIC TESTS

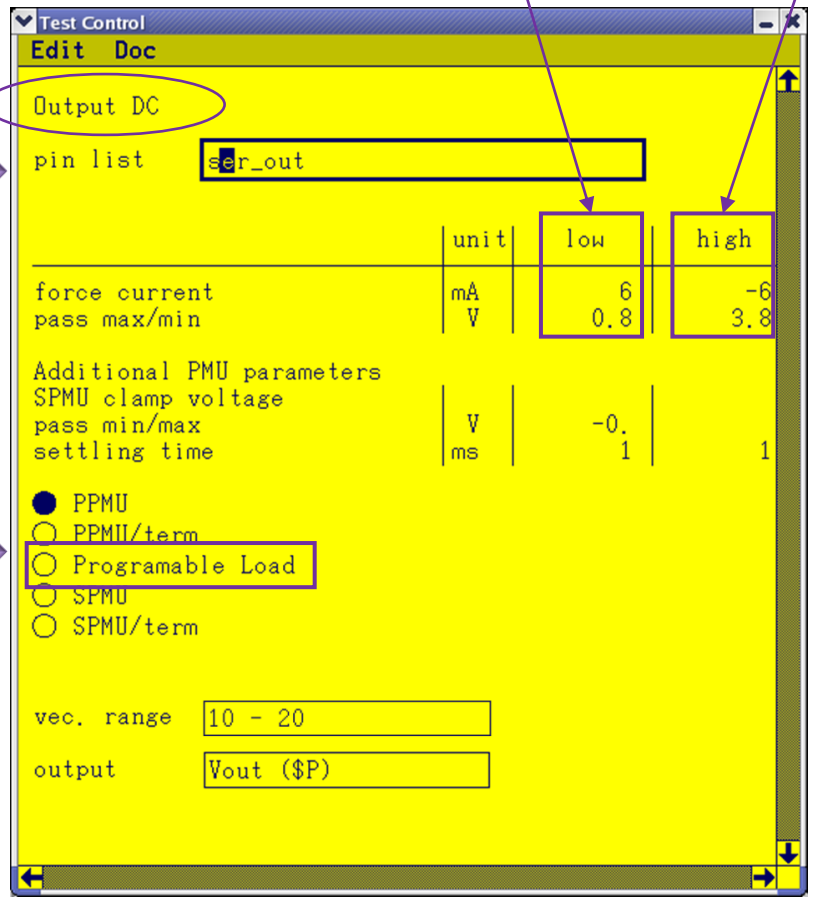
V_{OL}/V_{OH} TEST IN SMARTEST

Test Function: 'Output DC'

I_{OL}/V_{OL} I_{OH}/V_{OH}

Pin list

Instrument

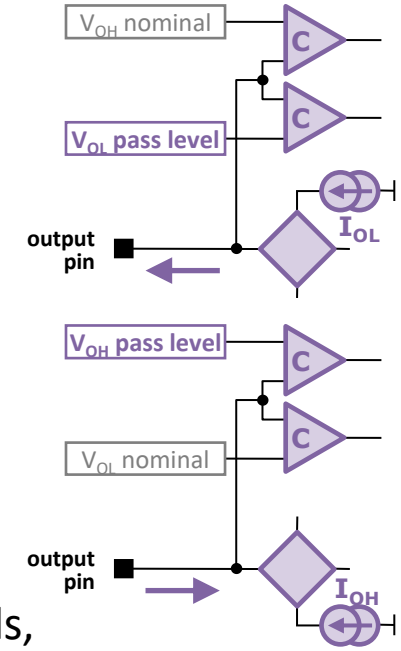


Test Procedure with PL option

1. Set V_{OL} to low pass level
   Set active load to I_{OL}
   Execute functional test

2. Set back V_{OL} to nominal level
   Set V_{OH} to high pass level
   Set active load to I_{OH}
   Execute functional test

3. Return FAIL if either execution fails, otherwise return PASS

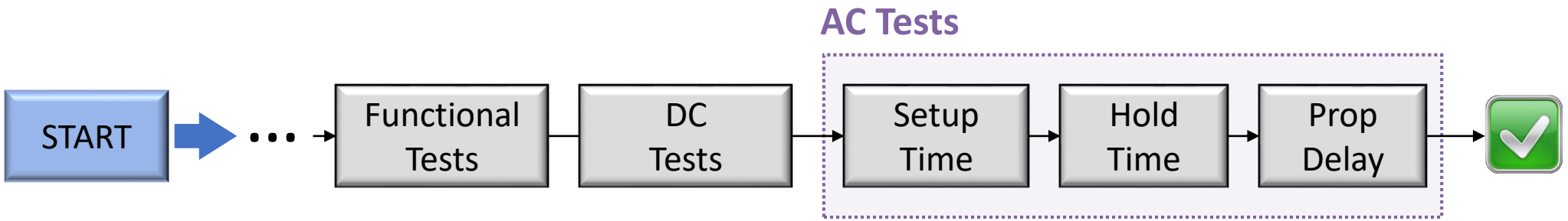


* *V_{OL}/V_{OH} measurement: iterations of steps 1 & 2 with incremental change of V_{OL}/V_{OH} setting to identify P/F transition (meas. value = last Pass value); Return FAIL if measured V_{OL} > low pass level or measured V_{OH} < high pass level, otherwise return PASS*

TEST METHODS: AC PARAMETRIC TESTS

AC TESTS

- Purpose
  - Verify device AC performances, once functionality & DC performances are OK
- Classical Tests
  - Setup & hold times (inputs), propagation delay (outputs), frequency

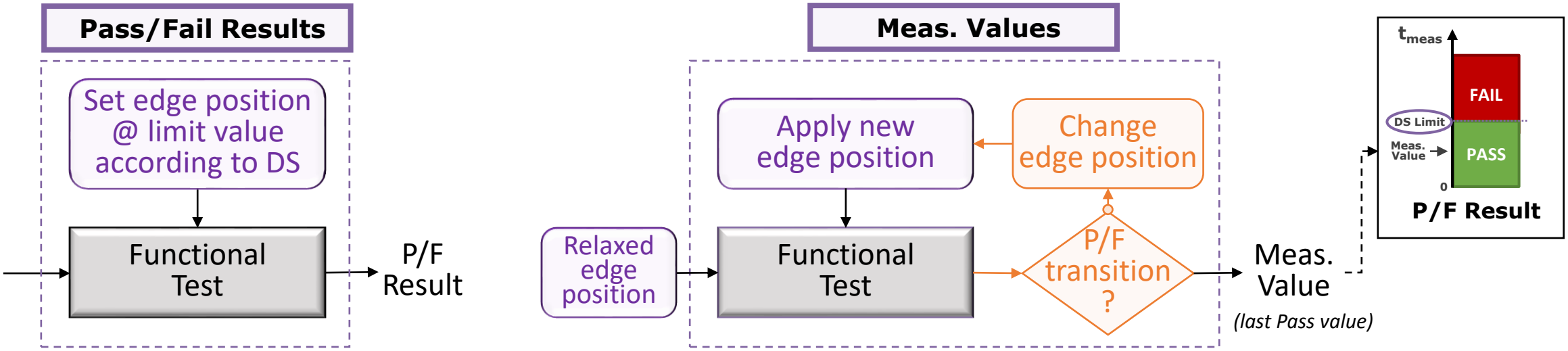


All AC tests are based on functional tests

TEST METHODS: AC PARAMETRIC TESTS

AC TESTS

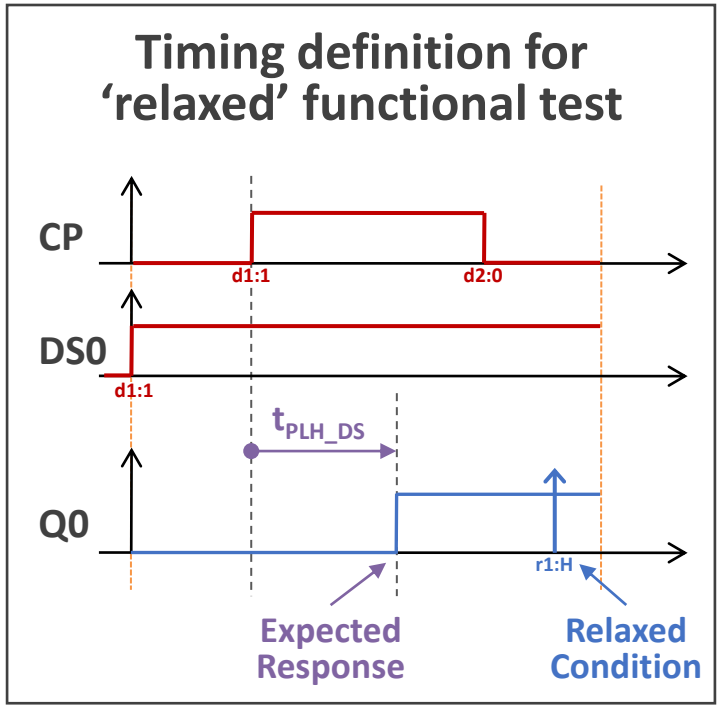
- Principle
  - Pass/Fail Results: one functional test performed with edge position set at limit value w.r.t. datasheet specification for the targeted performance
  - Measurement Values: iterations of functional test with changing of edge position in order to identify Pass/Fail transition (meas. value = last Pass value); Comparison of meas. value with datasheet specification to return a Pass/Fail result



5 Test Methods: AC Parametric Tests

AC Tests

- Illustration: t_{PLH}



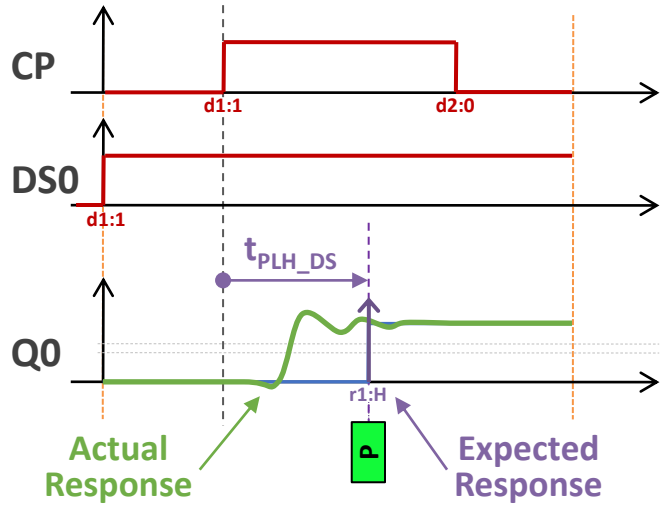
One functional test

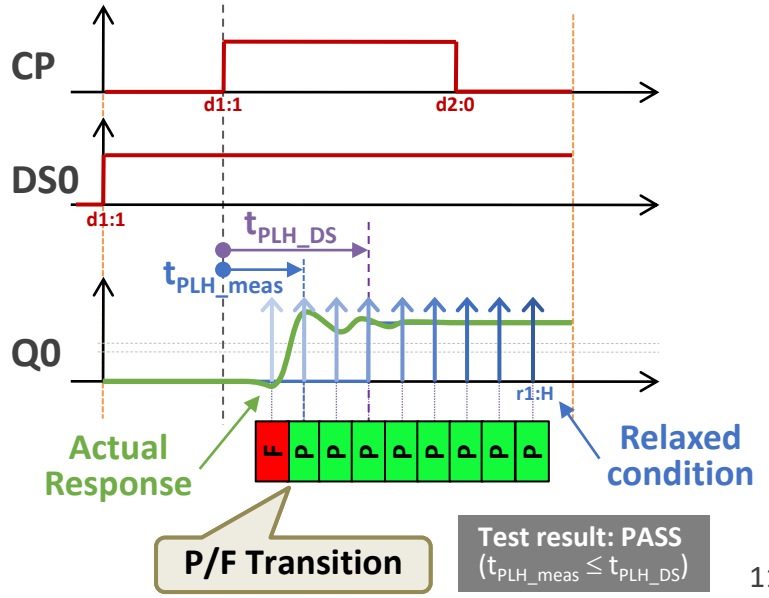
Pass/Fail Result

Iterations of functional test

Meas. Value
(last Pass value)

Prop Delay Test

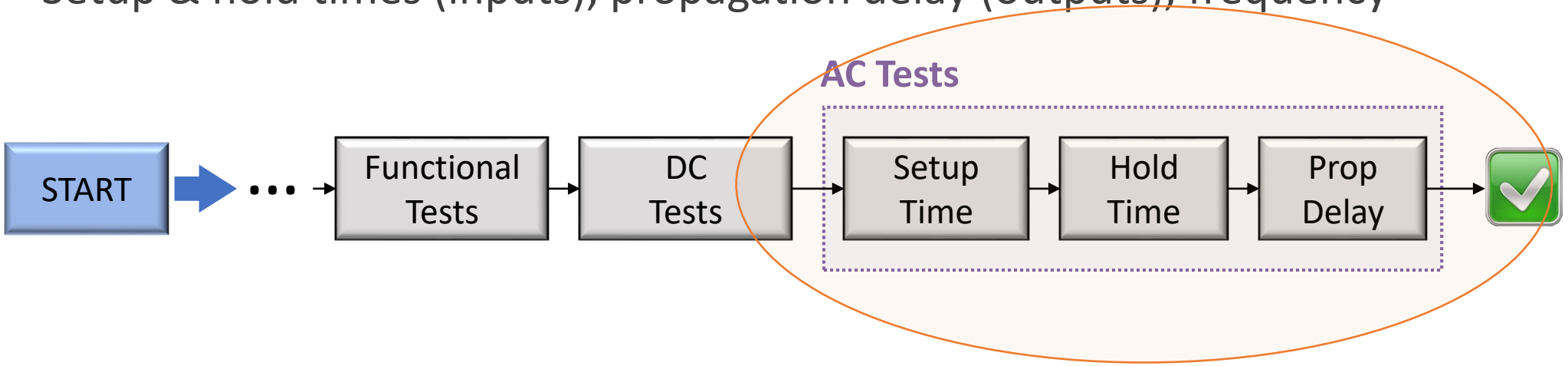




TEST METHODS: AC PARAMETRIC TESTS

AC TESTS

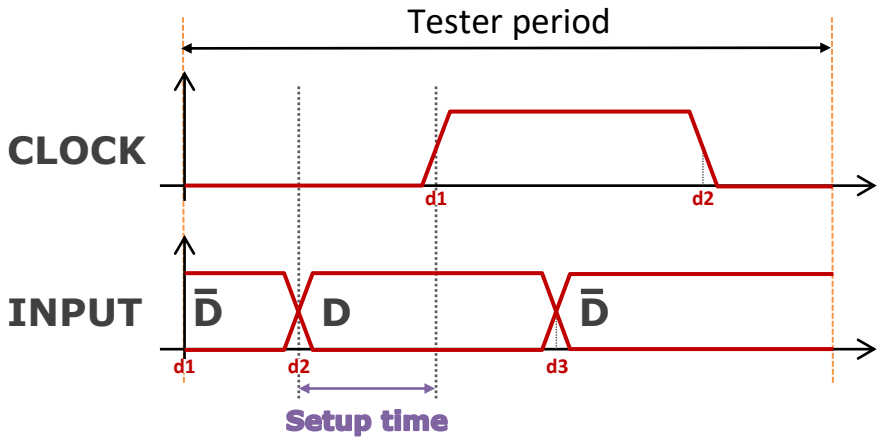
- Purpose
  - Verify device AC performances, once functionality & DC performances are OK
- Classical Tests
  - Setup & hold times (inputs), propagation delay (outputs), frequency



5 TEST METHODS: AC PARAMETRIC TESTS

SETUP TIME TEST

- Definition
  - Minimum amount of time the data input must be held steady before the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(*3 edges with SBC format to handle both setup & hold times*)

AC Operating Requirements for ACT

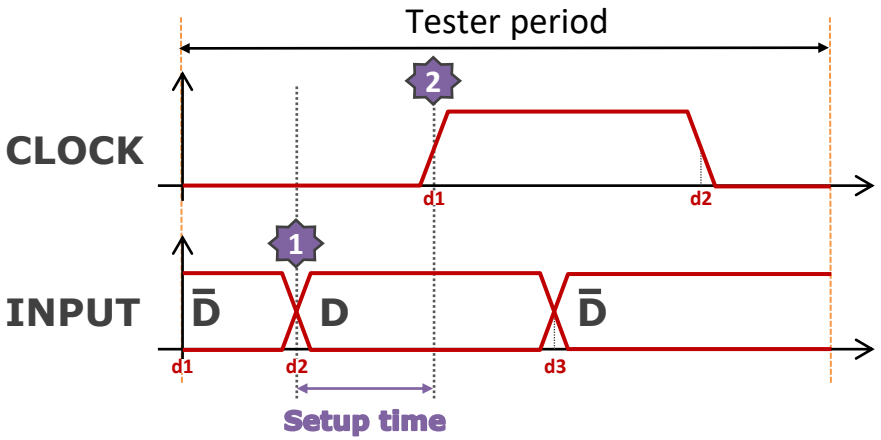
Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF Typ	$T_A = +25°C$, $C_L = 50$ pF Guaranteed Minimum	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
t_S	Setup Time, HIGH or LOW S_n or S_1 to CP	5.0	2.0	5.0	5.5	ns
t_H	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	−2.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.0	ns
t_H	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	−1.0	1.0	1.0	ns
t_W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns
t_W	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	3.5	ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	5.0	0	1.5	1.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

5 TEST METHODS: AC PARAMETRIC TESTS

SETUP TIME TEST IN SMARTEST

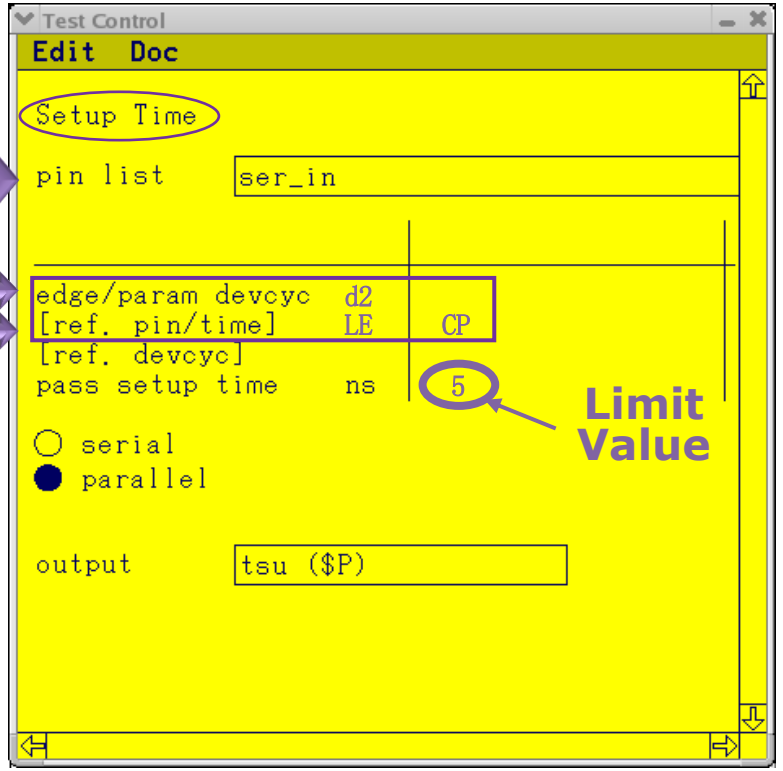
- Definition
  - Minimum amount of time the data input must be held steady before the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(*3 edges with SBC format to handle both setup & hold times*)

Test Function: 'Setup Time'

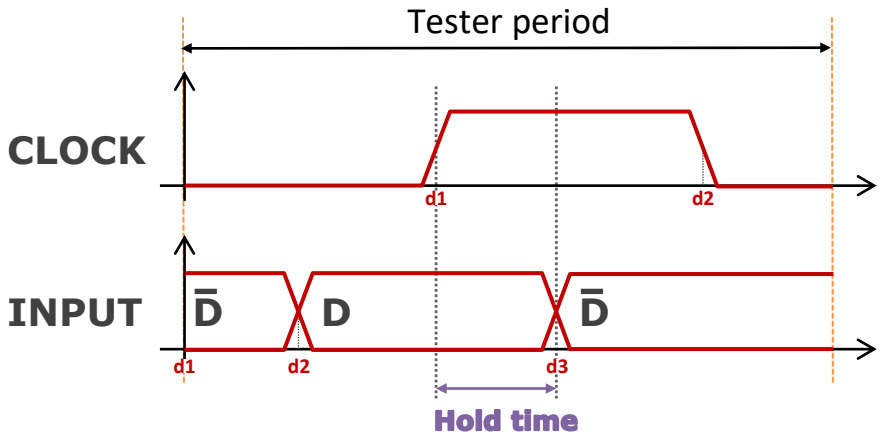
1 Edge under focus
2 Reference (*optional*)



TEST METHODS: AC PARAMETRIC TESTS

HOLD TIME TEST

- Definition
  - Minimum amount of time the data input must be held steady after the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(*3 edges with SBC format to handle both setup & hold times*)

AC Operating Requirements for ACT

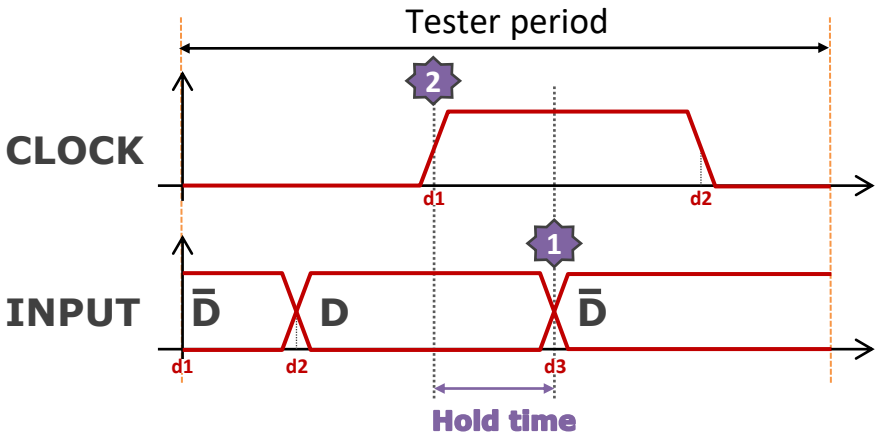
Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF Typ	$T_A = +25°C$, $C_L = 50$ pF Guaranteed Minimum	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Guaranteed Minimum	Units
t_S	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.5	ns
t_H	Hold Time, HIGH or LOW S_n or S_1 to CP	5.0	−2.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.0	ns
t_H	Hold Time, HIGH or LOW DS_n or DS_7 to CP	5.0	−1.0	1.0	1.0	ns
t_W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns
t_W	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	3.5	ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	5.0	0	1.5	1.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

5 Test Methods: AC Parametric Tests

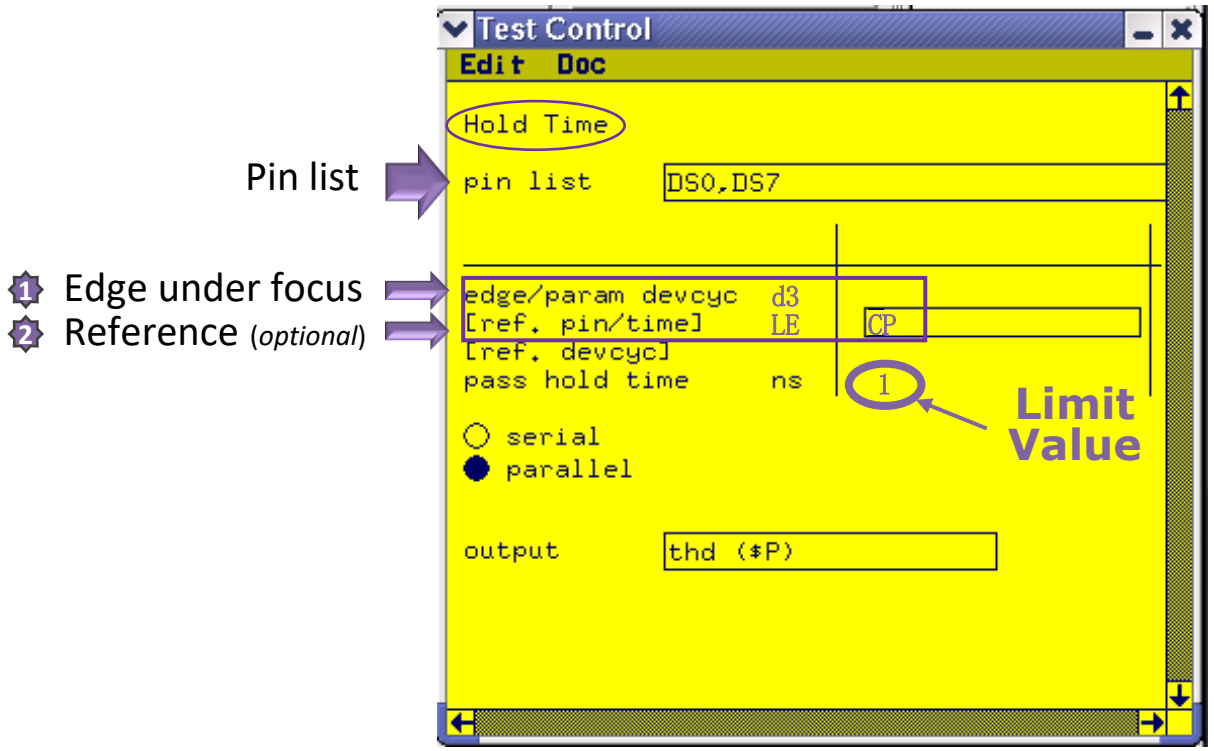
Hold Time Test in SmarTest

- Definition
  - Minimum amount of time the data input must be held steady after the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(*3 edges with SBC format to handle both setup & hold times*)

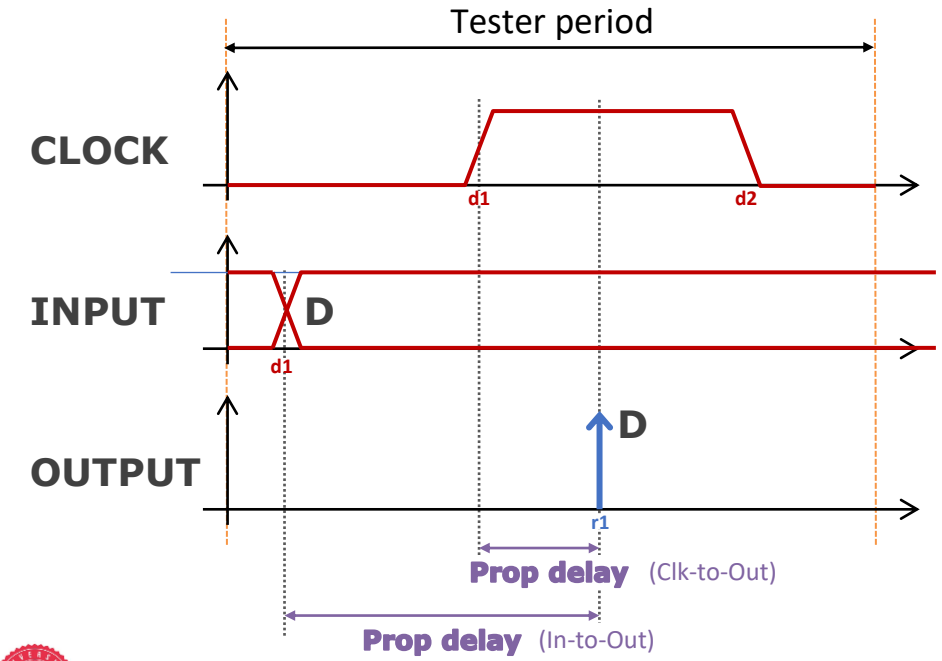
Test Function: 'Hold Time'



5 TEST METHODS: AC PARAMETRIC TESTS

PROPAGATION DELAY TEST

- Definition
  - Maximum amount of time that ensures the presence of the data after a transition of a reference signal (input or clock)
- Test performed on output pins only



AC Electrical Characteristics for ACT

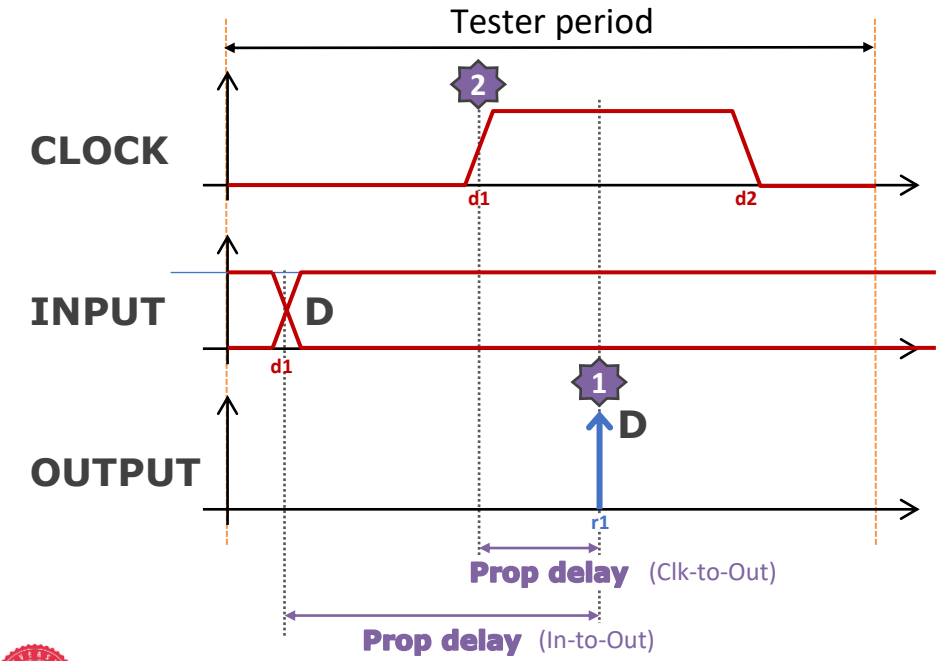
Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t_{PLH}	Propagation Delay CP to I/O_n	5.0	4.5	8.5	12.5	4.5	13.5	ns
t_{PHL}	Propagation Delay CP to I/O_n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	4.0	14.0	15.0	4.0	18.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0	4.0	13.0	14.5	3.5	17.5	ns

t_{PLH} & t_{PHL} might be different

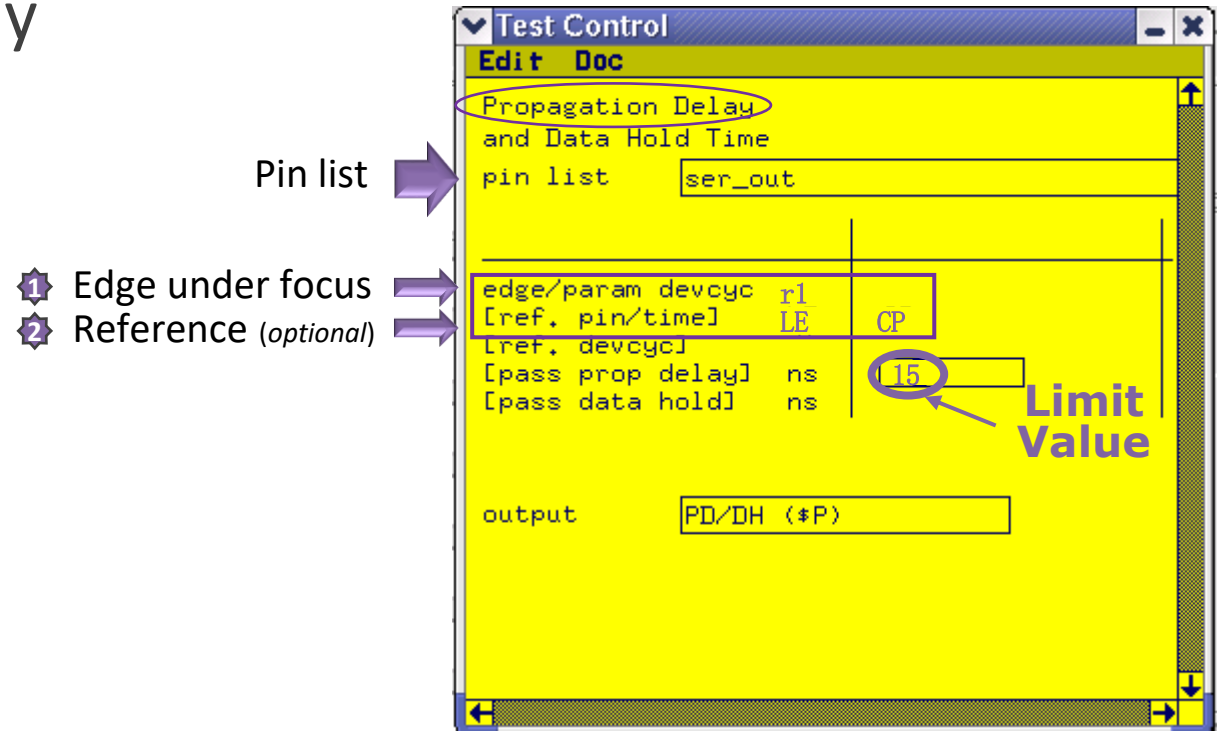
5 Test Methods: AC Parametric Tests

Propagation Delay Test in SmarTest

- Definition
  - Maximum amount of time that ensures the presence of the data after a transition of a reference signal (input or clock)
- Test performed on output pins only



Test Function: 'Prop Delay'

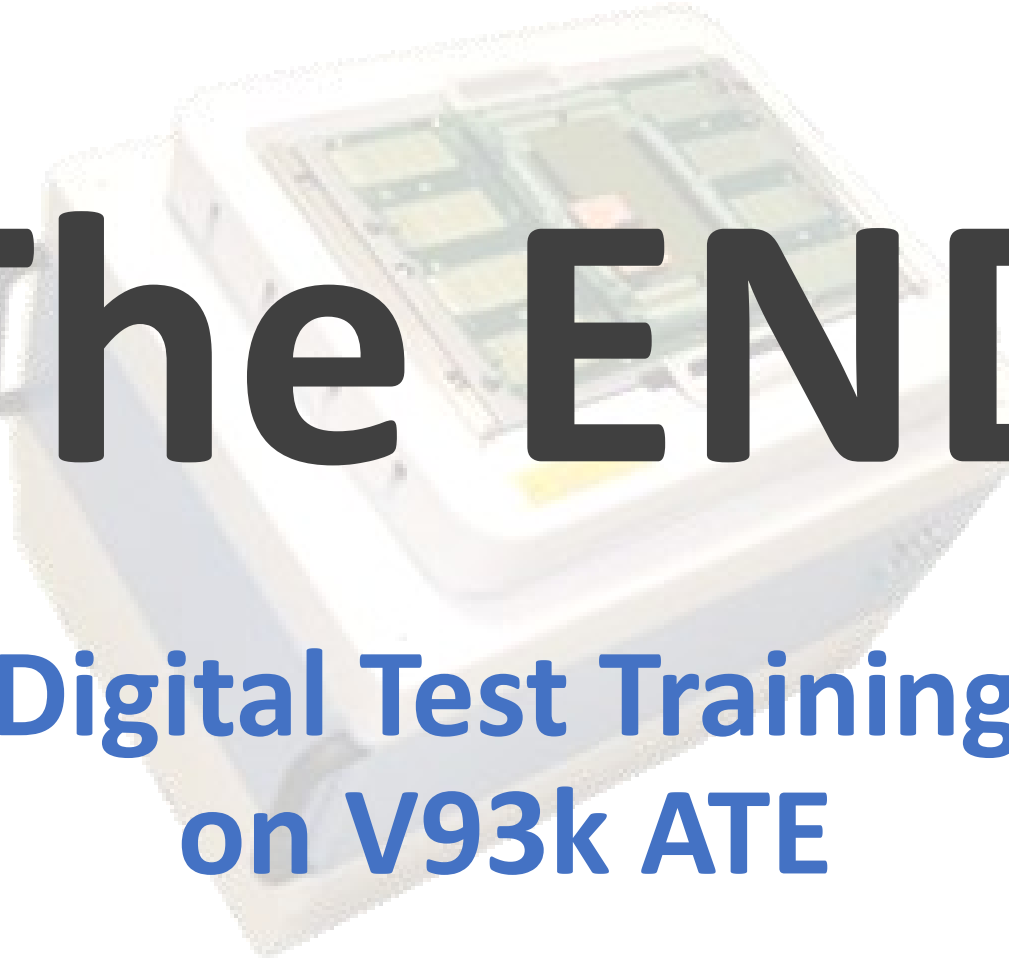


5

Lab & Exercises:

- **Implementation of Parametric Tests on 74ACT299** ***(off-line + on-line)***

- **Questions about Parametric Tests**



The END

Digital Test Training
on V93k ATE