

INDUSTRIAL TEST OF INTEGRATED CIRCUITS

Digital Test Training
on V93k ATE



M2 2024-25: ORGANIZATION

❖ Planning: 5 sessions

#	Date	Duration
1	September 9 th 14h00-15h30	1.5hrs
2	September 9 th 15h30-18h30	3hrs
3	September 23 rd 14h00-17h00	3hrs
4	September 30 th 14h00-17h00	3hrs
5	November 4 th 14h00-17h00	3hrs
Total		13.5hrs

❖ “Integrated course”

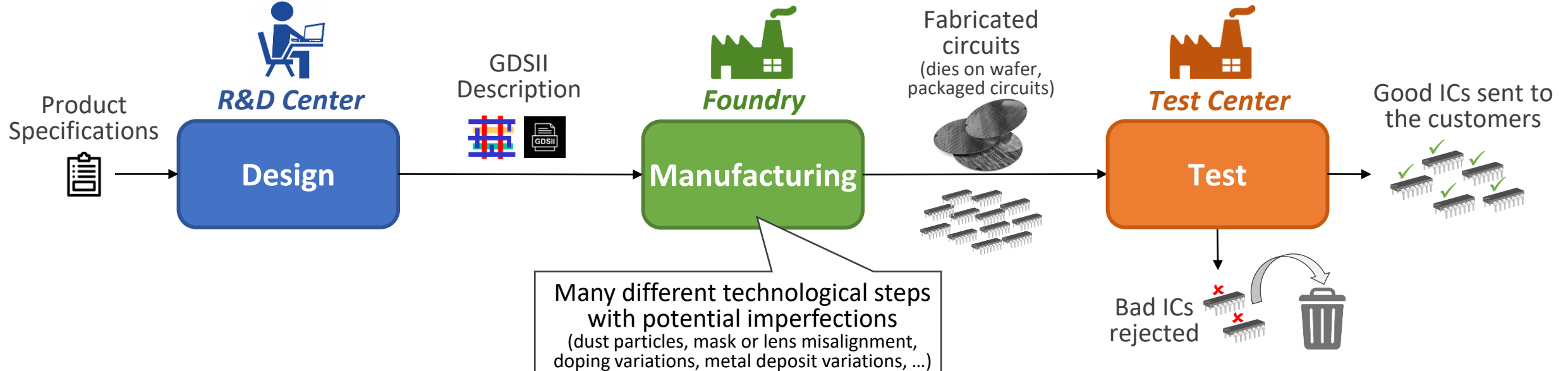
- Mix of lectures & labs/exercises during all sessions

❖ Evaluation

- No formal exam but continuous assessment
- Mini-tests performed during the sessions
- Final grade: Sum of mini-test scores

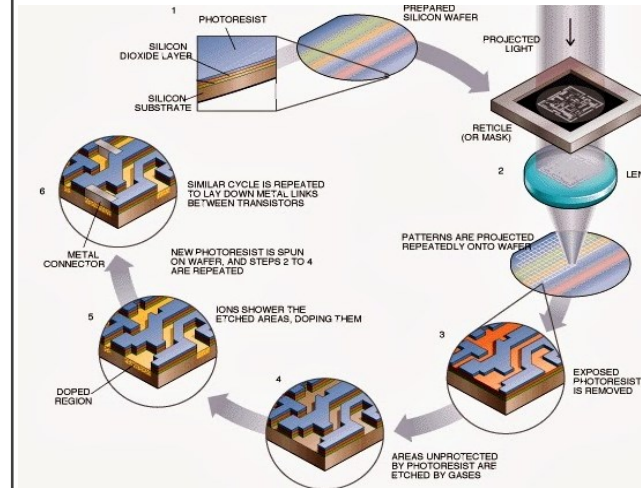
CONTEXT

❖ Major steps in the production of Integrated Circuits



Why
Testing?

Many different technological steps with potential imperfections (dust particles, mask or lens misalignment, doping variations, metal deposit variations, ...)



➡ Test is an essential step as it guarantees the quality of the ICs delivered to the customers

OBJECTIVE OF THIS COURSE

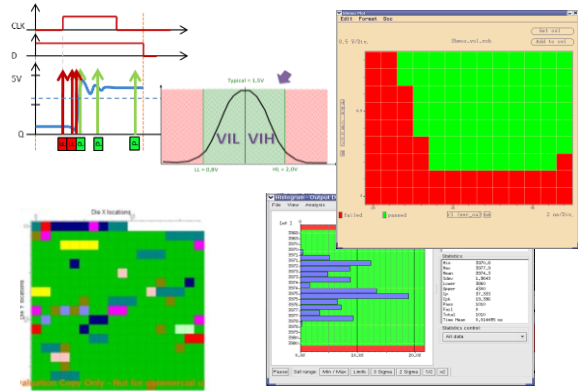


- Acquire the fundamentals of digital ICs **industrial testing**

Pre-production (first thousands of pieces)

Characterization tests

- Measurement values



The diagrams show timing waveforms for CLK, D, and V5 signals. A VIL/VIH diagram shows voltage levels for low and high input states. Two heatmaps represent pass/fail results for different test sets.

Design & Manufacturing adjustments

Basis for mass-production test program

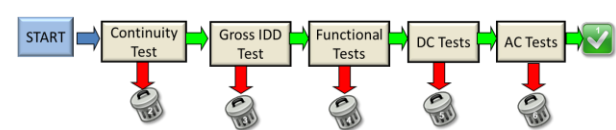
ATE



Mass-volume production (further millions of pieces)

Go/no-go tests

- Pass/Fail results



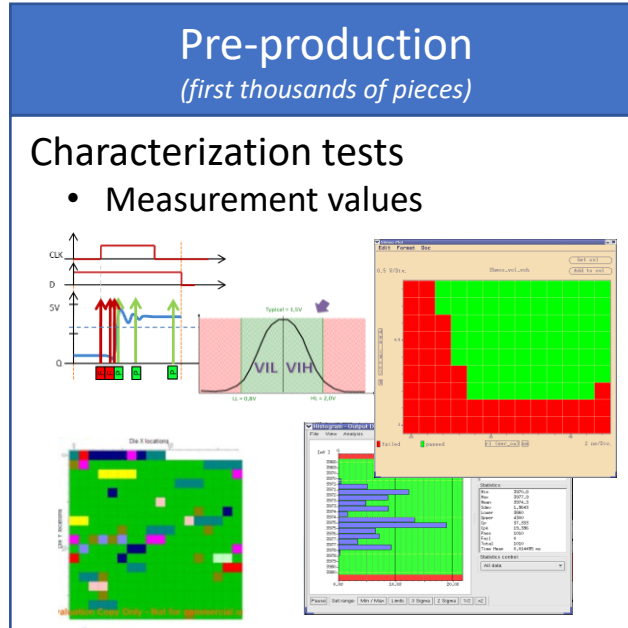
The flowchart shows the sequence of tests for mass-volume production: START, Continuity Test, Gross IDD Test, Functional Tests, DC Tests, AC Tests, and finally PASS. Each test step is represented by a box with a corresponding icon (e.g., a chip for Continuity Test, a chip with a red arrow for Gross IDD Test, a chip with a green arrow for Functional Tests, a chip with a red arrow for DC Tests, and a chip with a green arrow for AC Tests). A green checkmark indicates the final PASS result.

Test time: major factor contributing to the testing costs

Responsible for the quality of devices sent to customers

OBJECTIVE OF THIS COURSE

- Acquire the **fundamentals** of digital ICs **industrial testing**



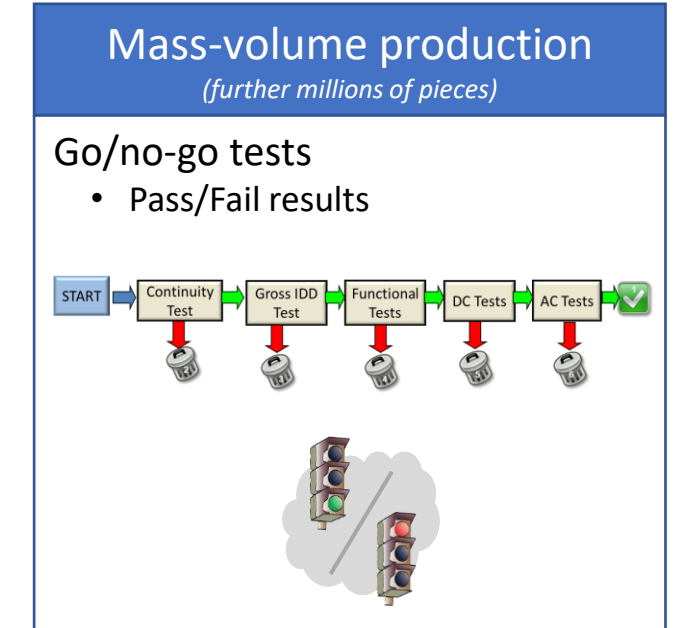
Design & Manufacturing adjustments

Basis for mass-production test program



Concepts

- ❖ Equipment
 - HW: Physical resources of the ATE
 - SW: Tools to control the ATE
- ❖ Test Program
 - Test methods
 - Test flow
 - Test results analysis
 - Debug & diagnosis



Test time: major factor contributing to the testing costs

Responsible for the quality of devices sent to customers

INDUSTRIAL ENVIRONMENT

- Automatic Test Equipment (ATE)



TERADYNE LTXredence ADVANTEST. VERIGY

Test Floor

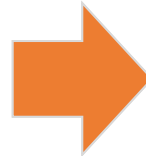


TARGETED COMPETENCIES

Key Learnings

Concepts

- ❖ Equipment
 - HW: Physical resources of the ATE
 - SW: Tools to control the ATE
- ❖ Test Program
 - Test methods
 - Test flow
 - Test results analysis
 - Debug & diagnosis



Practical Implementation

Digital IC



74ACT299:
8-bit shift/storage register



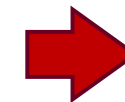
CNFM tester:
V93K



PASS

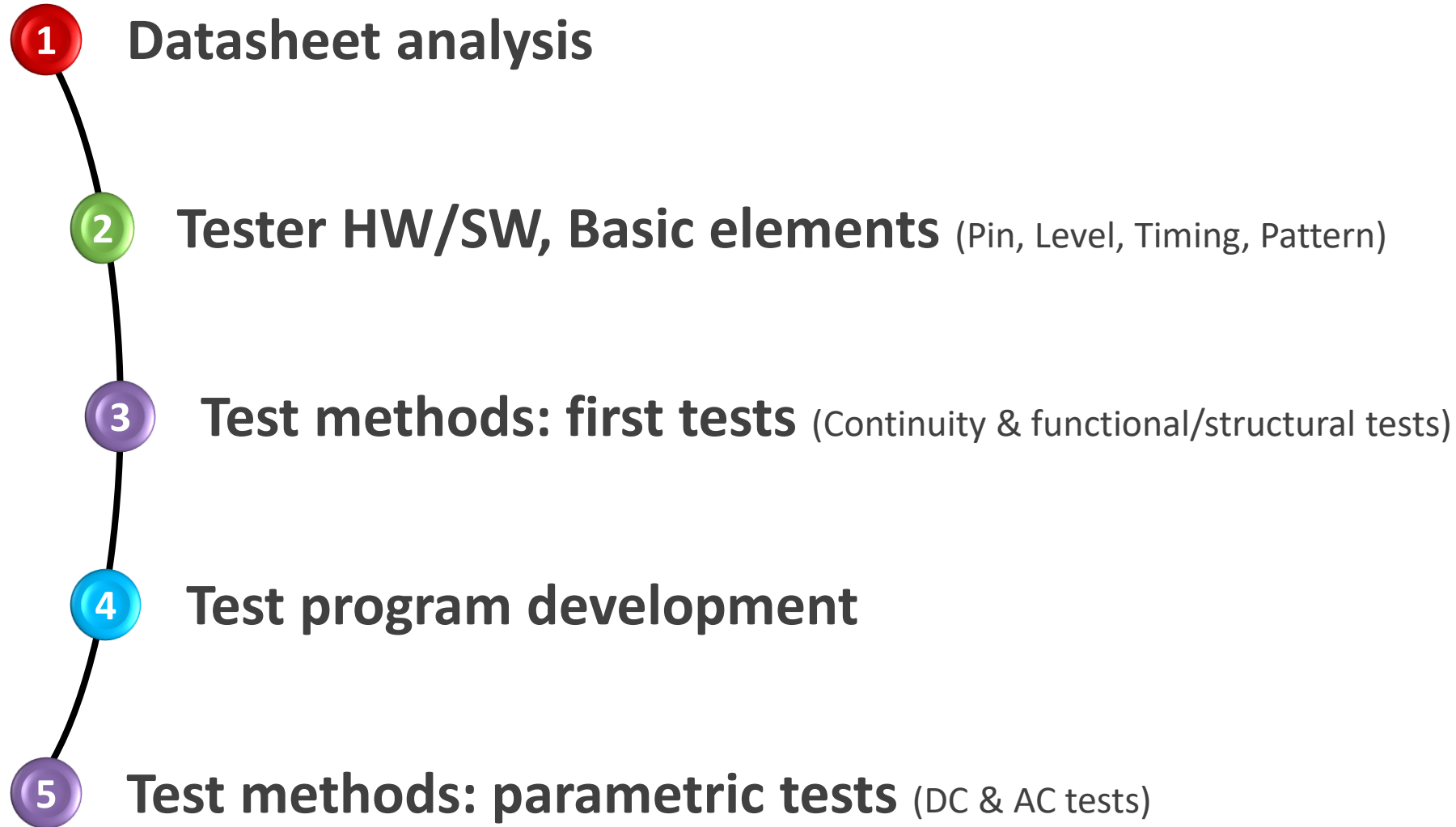


Functionality &
Performances



FAIL

LEARNING STEPS



PART 1

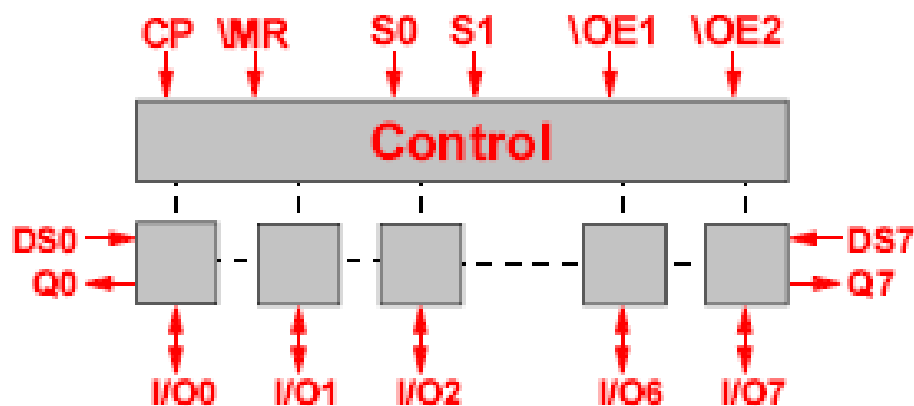


- **Device pins**
- **Functionality**
- **Operating conditions**
- **Performances** (typical/guaranteed limits)

1 DATASHEET ANALYSIS

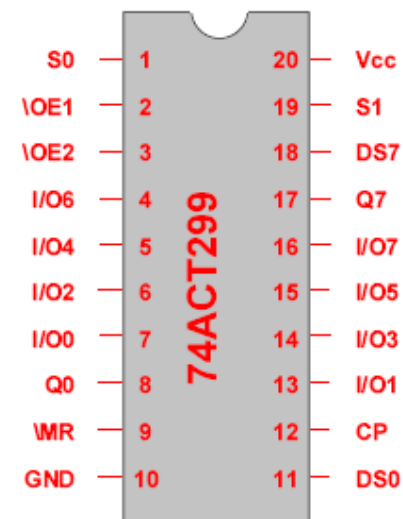
DEVICE UNDER TEST: 74ACT299

8- I/O universal shift/storage register



Pin Names	Description
CP	Clock Pulse Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE_1}$, $\overline{OE_2}$	TRI-STATE Output Enable Inputs
I/O ₀ –I/O ₇	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q ₀ , Q ₇	Serial Outputs

Pin Assignment



➡ Basis to define pin configuration

FUNCTIONALITY: TRUTH TABLE

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0-Q_7 = \text{LOW}$
H	H	H	$\nearrow$	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	$\nearrow$	Shift Right; $DS_0 \rightarrow Q_0, Q_0 \rightarrow Q_1, \text{etc.}$
H	H	L	$\nearrow$	Shift Left, $DS_7 \rightarrow Q_7, Q_7 \rightarrow Q_6, \text{etc.}$
H	L	L	X	Hold

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$\nearrow$ = LOW-to-HIGH Transition

- 4 Modes of operations controlled by (S_1, S_0)
 - Parallel Load: $(S_1, S_0) = 11$
 - Shift Right: $(S_1, S_0) = 01$
 - Shift Left: $(S_1, S_0) = 10$
 - Hold: $(S_1, S_0) = 00$
- Asynchronous reset controlled by $\overline{MR}$
 - active on $\overline{MR} = 0$

 **Basis to develop functional test pattern**

FROM DATA SHEET TO FUNCTIONAL TEST PATTERN

- Principle: Use of the truth table to define a test pattern (sequence of test vectors)
- Objective: Define a test pattern that checks all functionalities

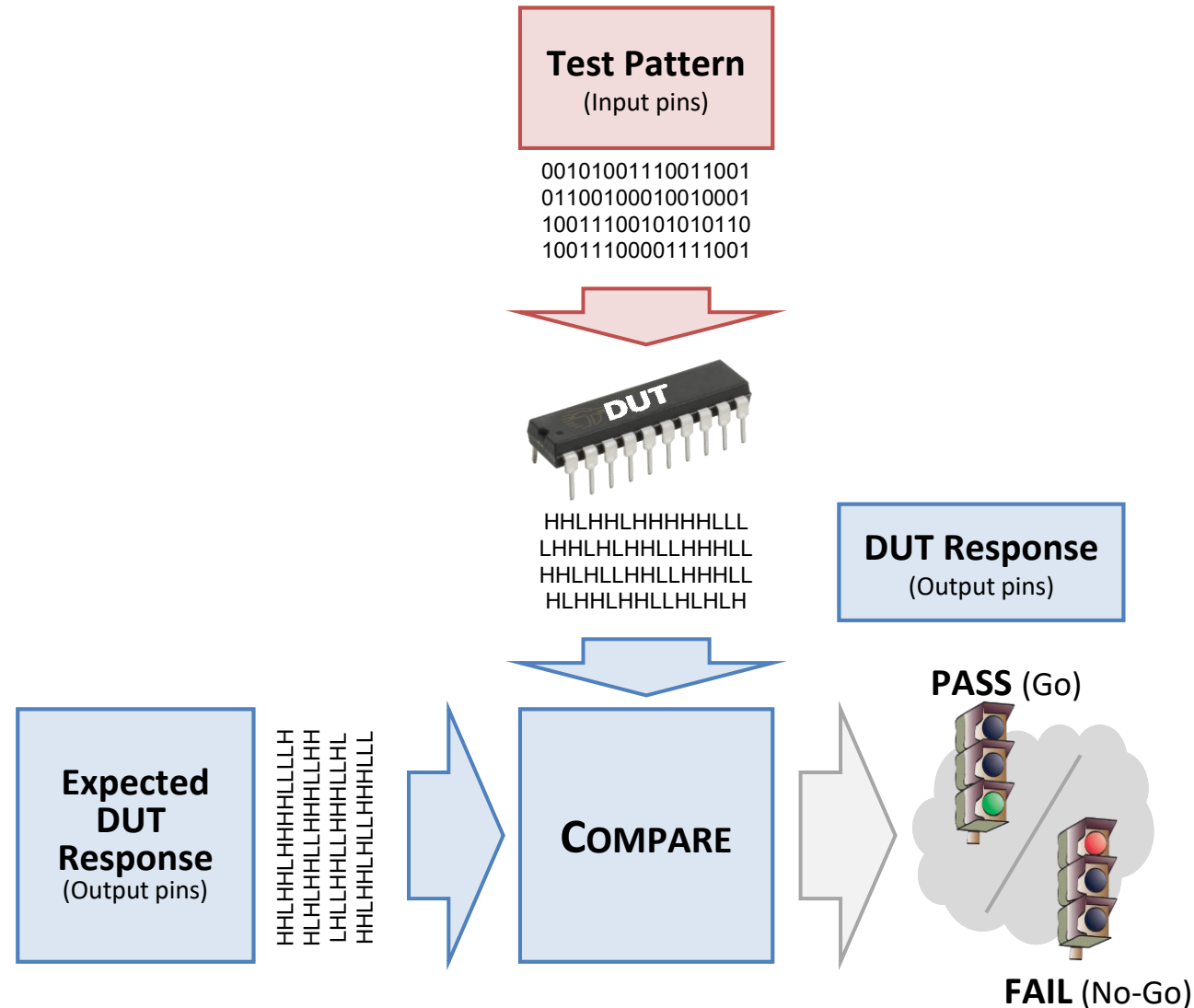
Inputs				Response
MR	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ –Q ₇ = LOW
H	H	H	↘	Parallel Load; I/O _n → Q _n
H	L	H	↘	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	↘	Shift Left, DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

Master reset
Hold
Parallel Load (10000000)
Hold
Shift Right x8 – DS0=0
Parallel Load (01010101)
Shift Left x8 – DS7=1
 ...

M	C	S	S	D	D	I	I	I	I	I	I	I	I	Q	Q	INSTRUCTIONS
R	P	0	1	S	S	O	O	O	O	O	O	O	O	0	7	
0	1	1	0	0	1	1	1	1	1	1	1	1	1	X	X	Master Reset
1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L	Hold
1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L	Parallel load
1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L	Shift right
1	1	1	0	0	0	L	L	L	L	L	L	H	L	H	H	Shift right
1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L	Shift right
1	1	1	1	0	0	0	1	0	1	0	1	0	1	L	H	Parallel load
1	1	0	1	0	1	H	L	H	L	H	L	H	H	H	H	Shift left

FUNCTIONAL TEST CONCEPT

Test Result:
No Measurement Value
Only Pass/Fail



OPERATING CONDITIONS

DATA SHEET

Recommended Operating Conditions

Supply Voltage (V_{CC})
(Unless Otherwise Specified)

'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)

74AC/ACT	-40°C to $+85^{\circ}\text{C}$
54AC/ACT	-55°C to $+125^{\circ}\text{C}$

Minimum Input Edge Rate ($\Delta V/\Delta t$)

'AC Devices

V_{IN} from 30% to 70% of V_{CC}

V_{CC} @ 3.3V, 4.5V, 5.5V

125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)

'ACT Devices

V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V

125 mV/ns

TEST CONDITIONS FOR FUNCTIONAL TESTS

■ Supply Voltage (V_{CC})

- V_{CC} min = 4.5V *
- V_{CC} nom = 4.75V *
- V_{CC} max = 5.0V *

■ Operating Temperature

- Cold: -40°C
- Room: $+25^{\circ}\text{C}$ *
- Hot: $+85^{\circ}\text{C}$ *

* Production Test

PERFORMANCES

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT	Units	Conditions
			T _A = 25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} −24 mA −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND
I _{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±5.5	±3.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

CLASSICAL PARAMETRIC DC TESTS

- Voltage
 - Input pins: V_{IH}/V_{IL}
 - Output pins: V_{OH}/V_{OL}
- Current
 - Input pins: I_{IN} (leakage)
 - Supply: I_{CC} (consumption)

Limit values for parametric DC tests
(& test conditions)

PERFORMANCES

AC Electrical Characteristics for ACT

(Outputs)

Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t _{FHL}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t _{PLH}	Propagation Delay CP to I/O _n	5.0	4.5	8.5	12.5	4.5	13.5	ns
t _{FHL}	Propagation Delay CP to I/O _n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t _{FHL}	Propagation Delay MR to Q ₀ or Q ₇	5.0	4.0	14.0	15.0	4.0	18.0	ns

AC Operating Requirements for ACT

(Inputs)

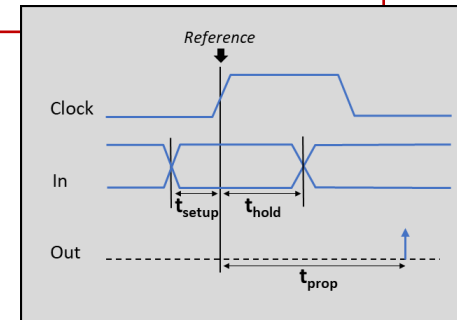
Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum			
t ₀	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.5		ns
t _H	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	-2.0	1.0	1.0		ns
t ₀	Setup Time, HIGH or LOW I/O _n to CP	5.0	1.5	4.0	4.5		ns
t _H	Hold Time, HIGH or LOW I/O _n to CP	5.0	-1.0	1.0	1.0		ns
t ₀	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	1.5	4.5	5.0		ns
t _H	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	-1.0	1.0	1.0		ns
t _W	CP Pulse Width HIGH or LOW						
t _W	MR Pulse Width, LOW						
t _{REC}	Recovery Time, MR to						

Note 9: Voltage Range 5.0 Is 5.1

Note 10: Voltage Range 5.0 Is 5.0V ± 0.5

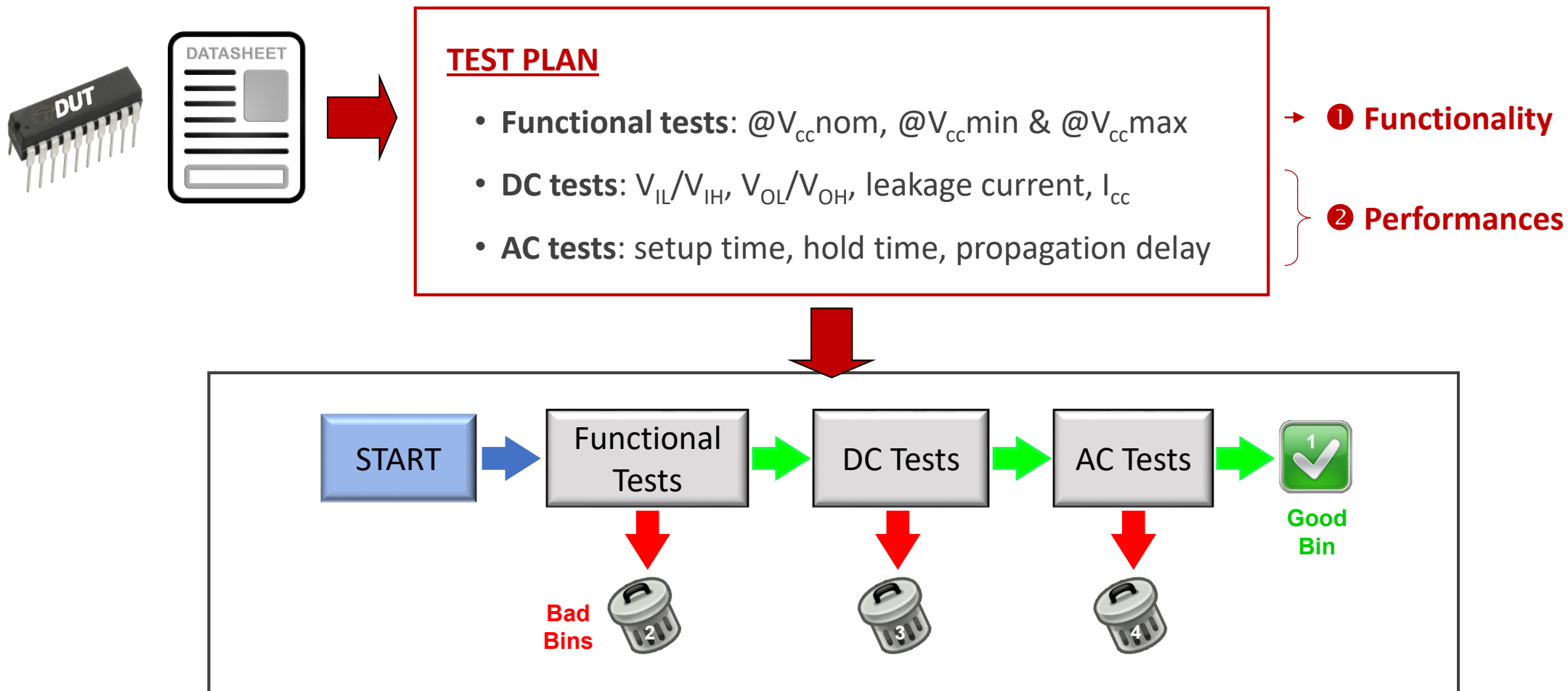
CLASSICAL PARAMETRIC AC TESTS

- Input pins
 - Setup Time
 - Hold Time
- Output pins
 - Propagation delay



Limit values for parametric AC tests
(test conditions)

SUMMARY: FROM DATASHEET TO TEST PLAN





Exercises:

74ACT299 Datasheet Analysis

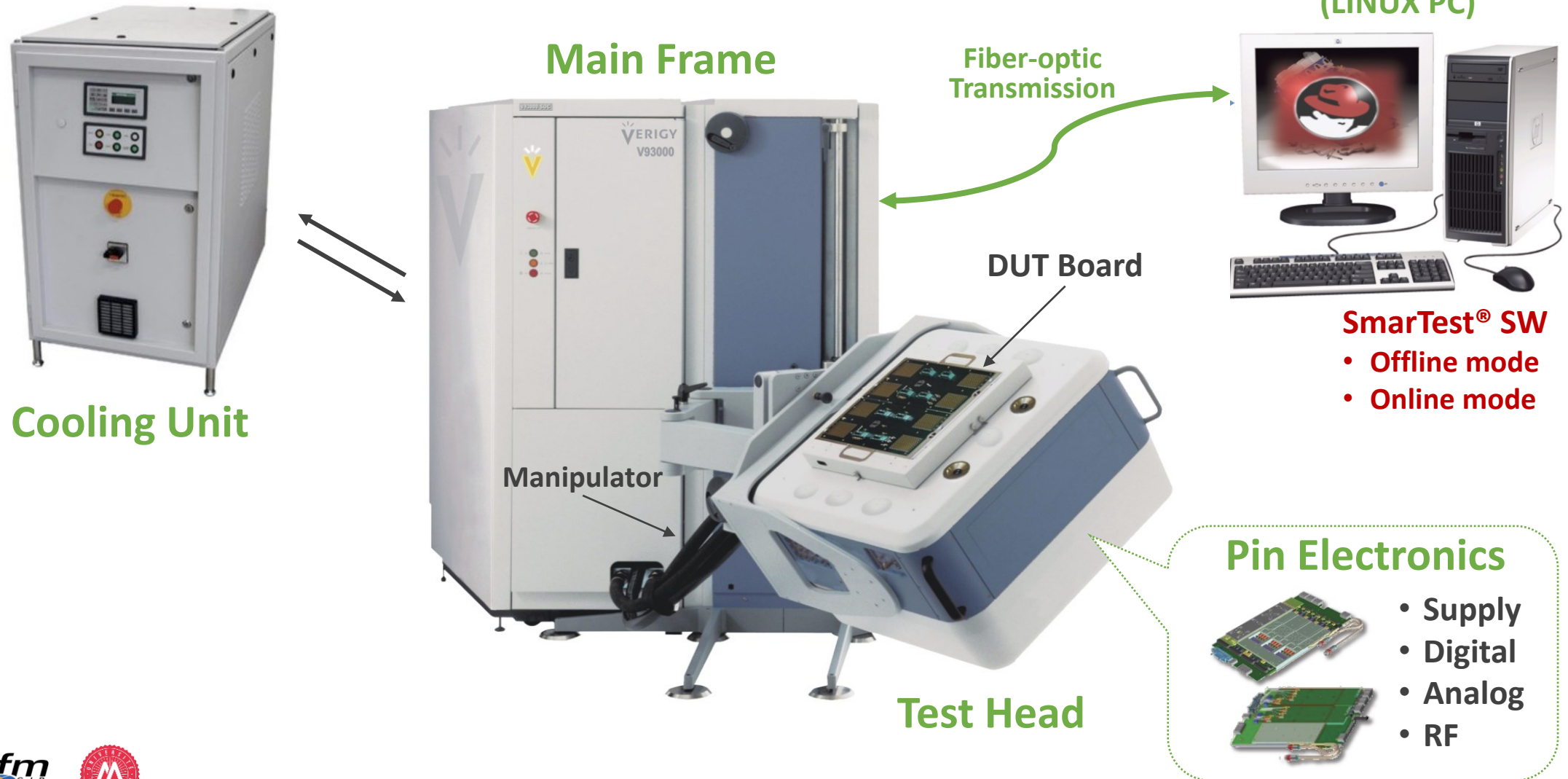


PART 2

TESTER
HW/SW
& BASIC
ELEMENTS

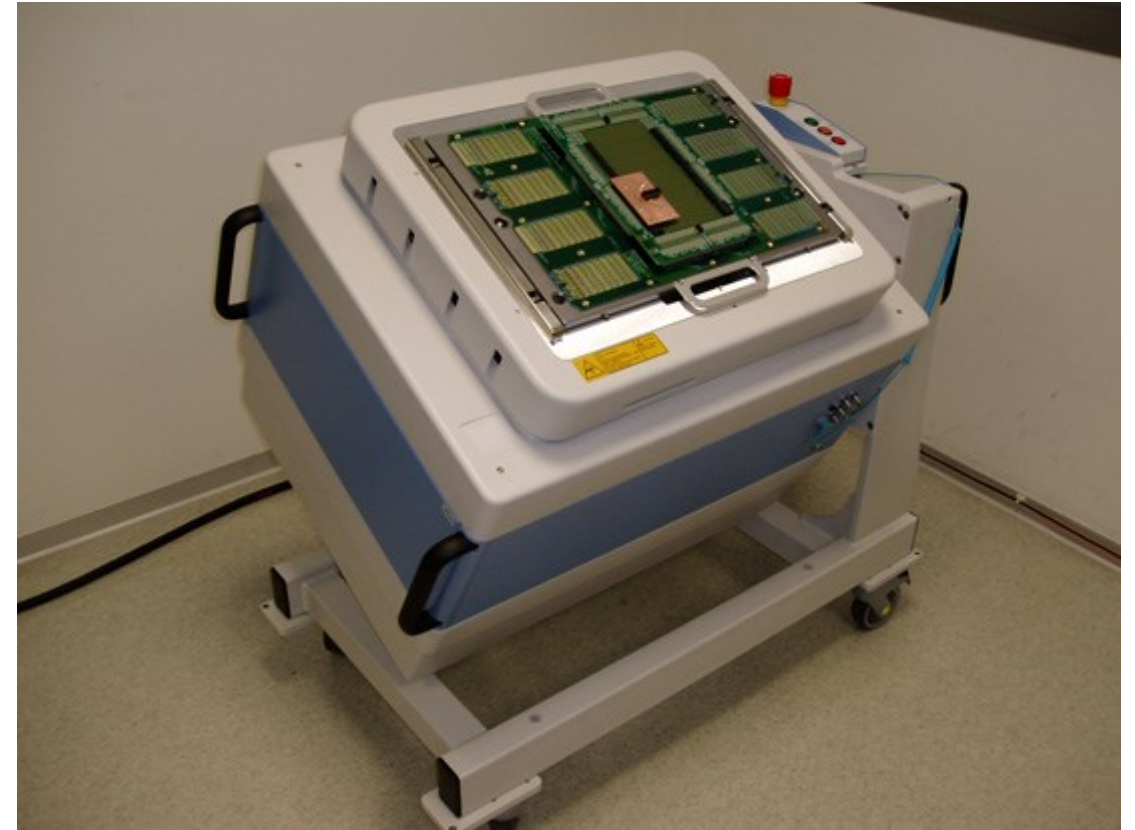
- HW resources
- SW interface
- Basic elements
 - Pin
 - Level
 - Timing
 - Pattern

OVERVIEW



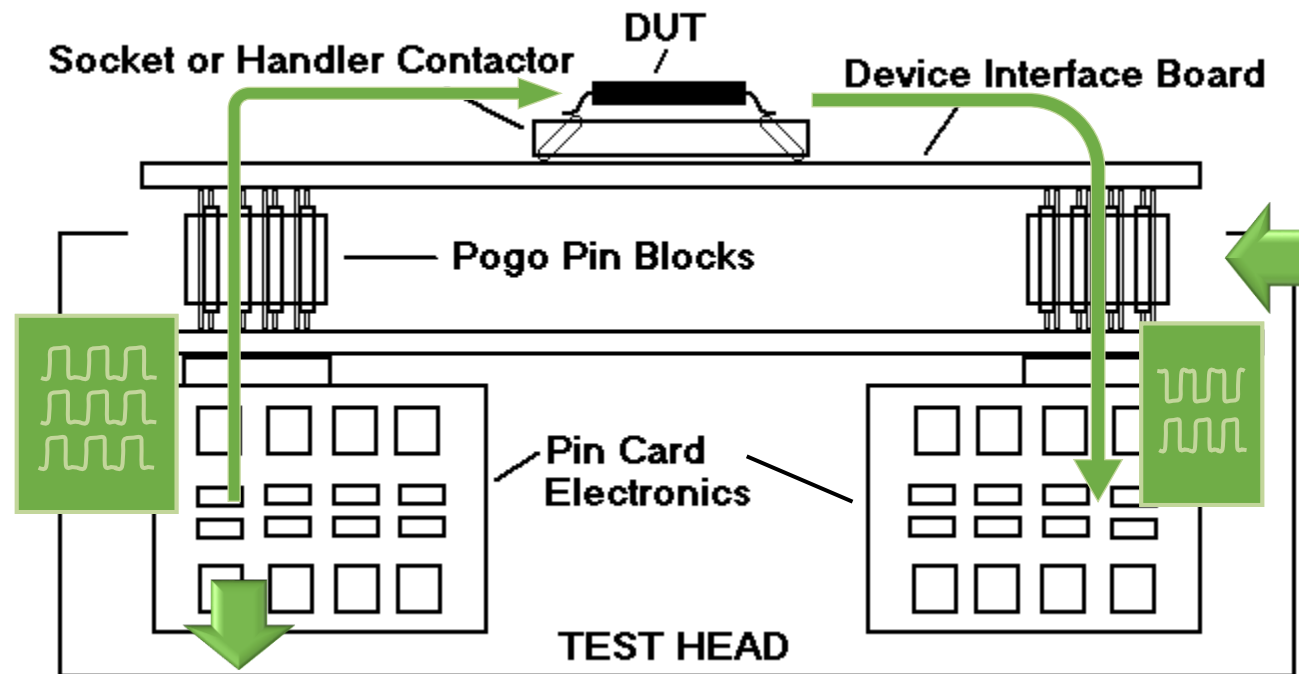
CNFM TESTER: COMPACT VERIGY V93K PINSCALE

- 64 Digital pins**
=> 200 Ks/s up to 3.6 Gs/s
- 8 Device Power Supply pins**
- 4 Analog Source pins**
=> Audio: 1.024 Msps, 24-bit
=> Video: 100 Msps, 14-bit
- 4 Analog Digitizer pins**
=> Audio: 200ksps, 24-bit, 50kHz BW
=> Video : 65Msps, 14-bit, 15MHz BW/100MHz

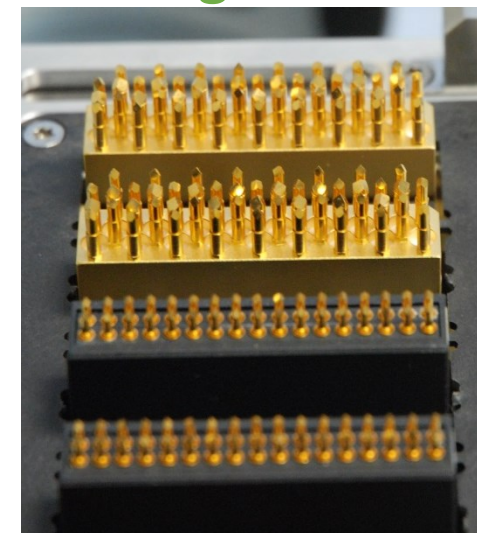




FROM TESTER TO DUT



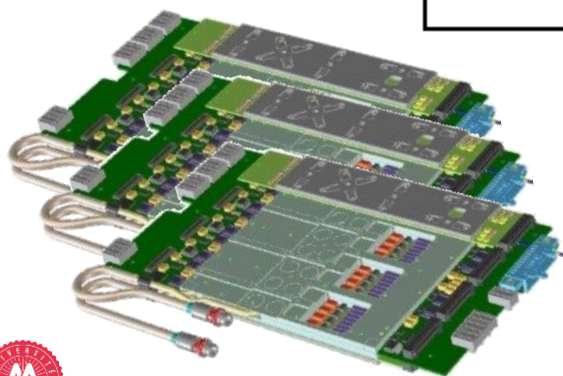
Pogo Pins



Pogo Pin:
Specific electrical connector with
an integrated helical string (high
durability and good resilience to
mechanical shock and vibration)

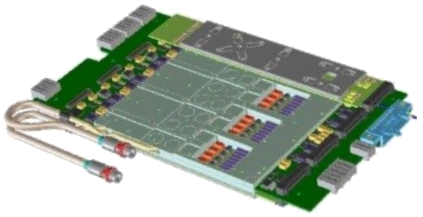
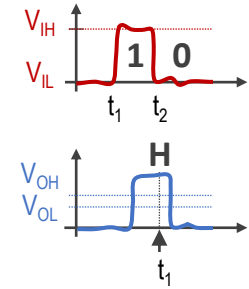


- Device Power Supply
- Clock board
- Pin Electronics (PE)

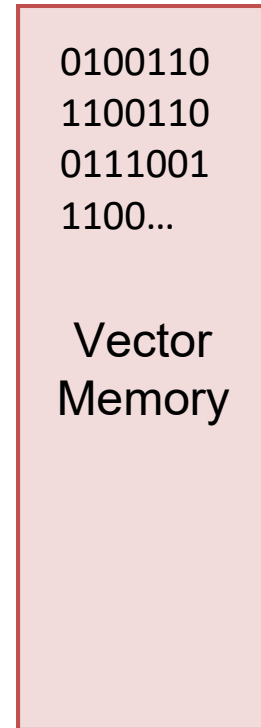


PIN ELECTRONICS

Electrical signal = Combination of level and timing information



PE



Test Processor

Timing
Generators

Waveform
Composer

Driver

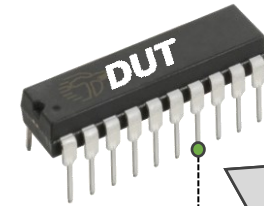
Receiver

PL

Prog.
Load

PMU

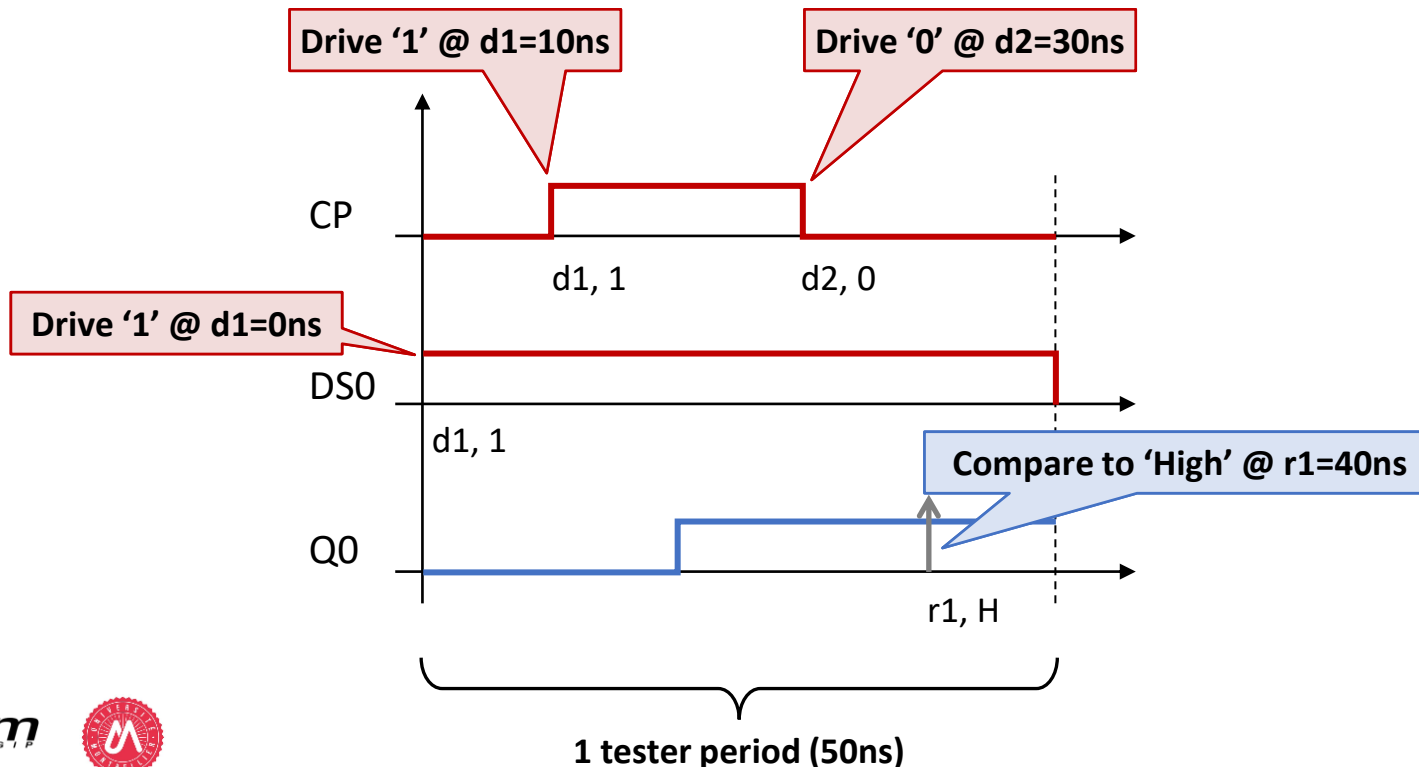
Parametric
Measurement
Unit



"PER PIN"
ARCHITECTURE

PIN ELECTRONICS - TIMING

- Concept
 - “actions” associated to “edges”
- Example



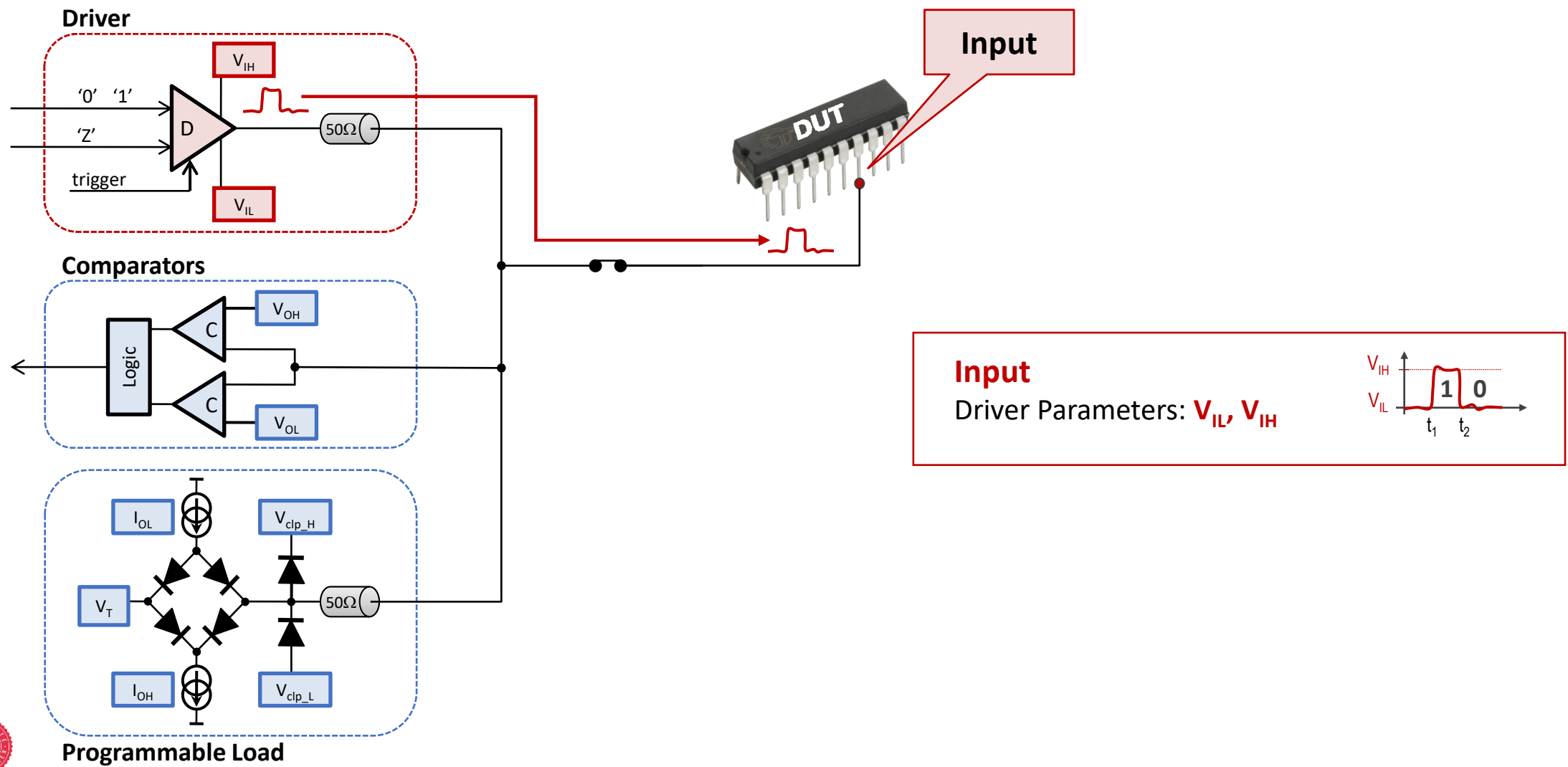
Tester timing resources per pin

- Input pins: 8 drive edges ($d1, d2, \dots, d8$)
- Output pins: 8 receive edges ($r1, r2, \dots, r8$)
- I/O pins: 8 drive edges + 8 receive edges

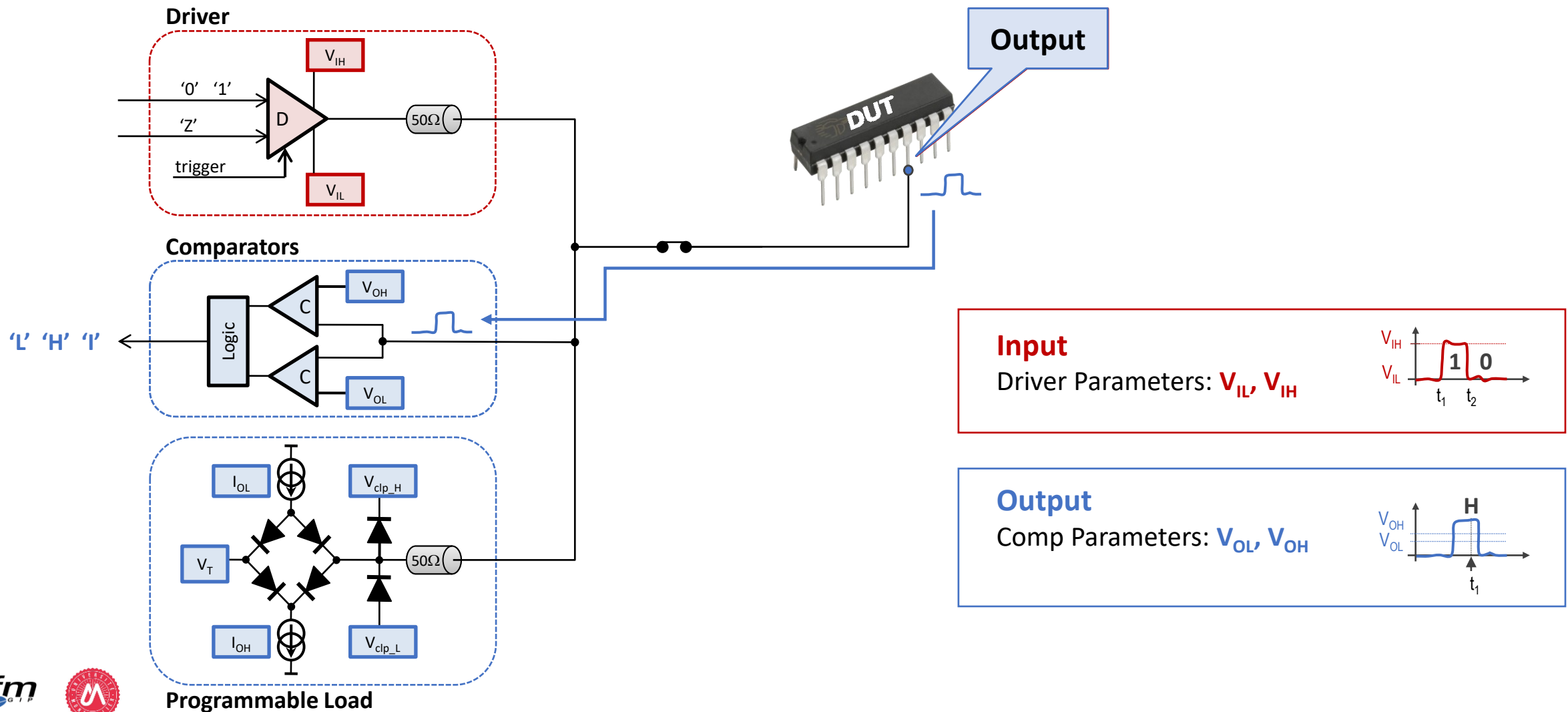
Actions

- Drive actions
 - 0: Drive '0'
 - 1: Drive '1'
 - Z: High impedance
 - N: No action
- Receive actions (*edges*)
 - L: Compare to 'Low'
 - H: Compare to 'High'
 - M: Compare to 'Intermediate'
 - X: Don't care

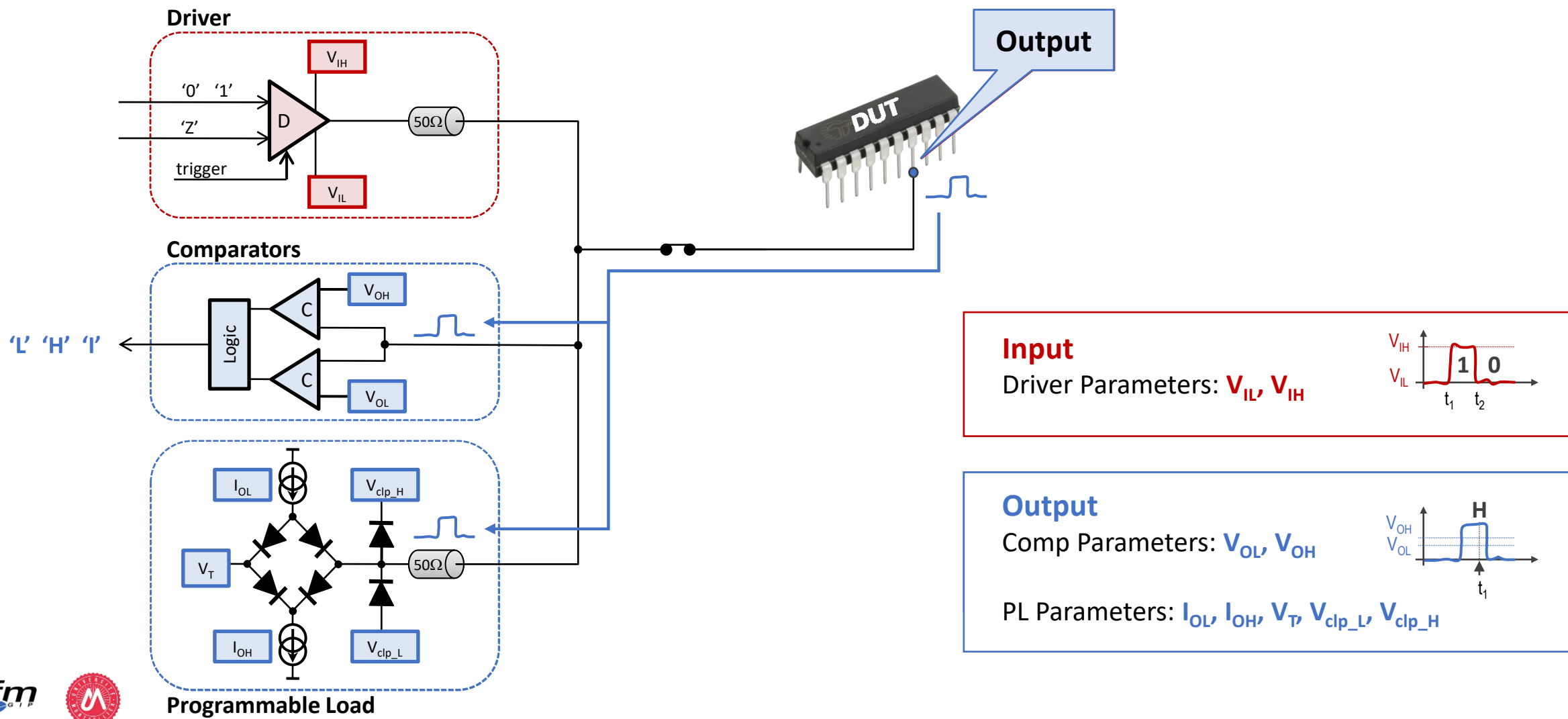
PIN ELECTRONICS - LEVEL



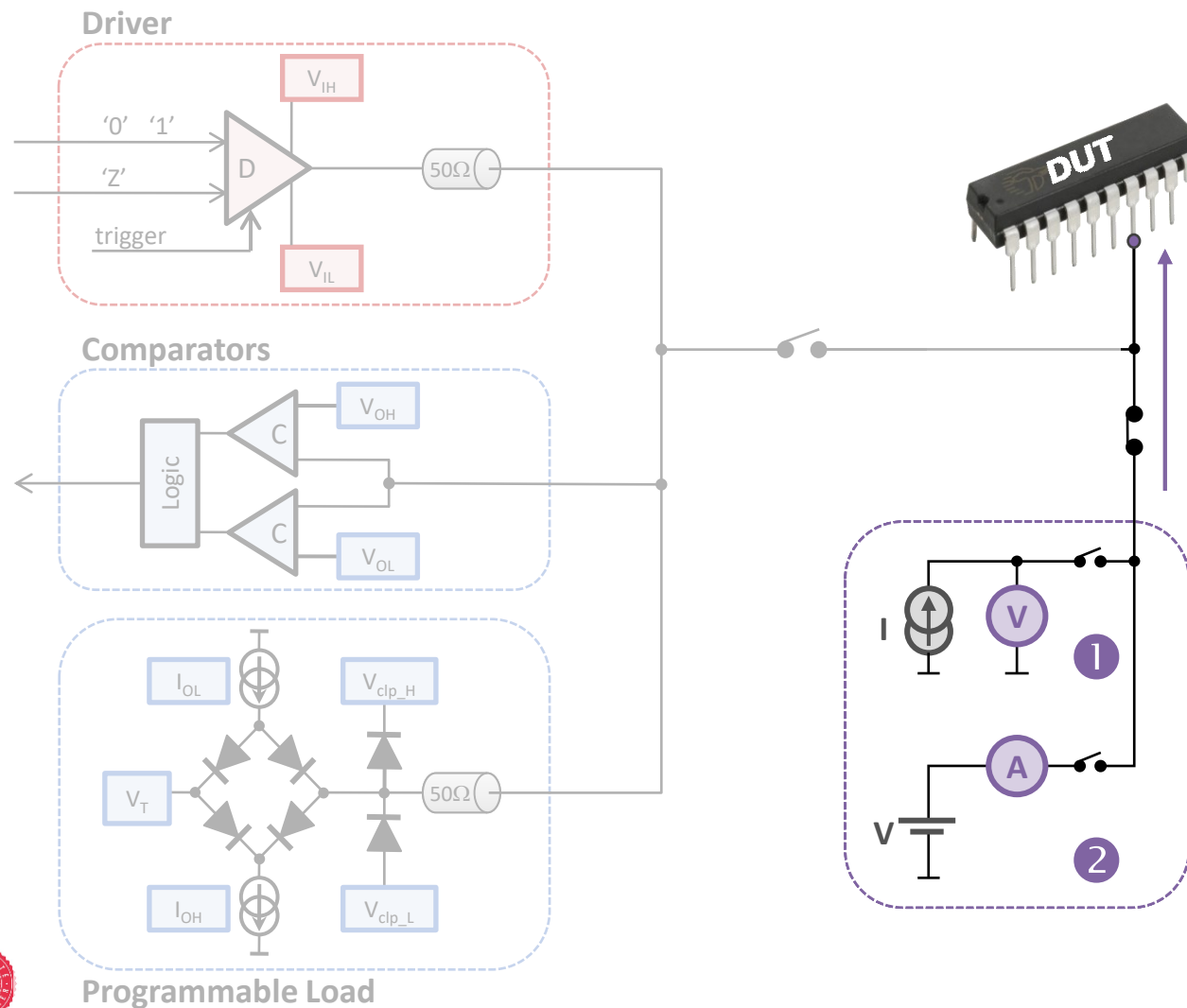
PIN ELECTRONICS - LEVEL



PIN ELECTRONICS - LEVEL



PIN ELECTRONICS - PMU

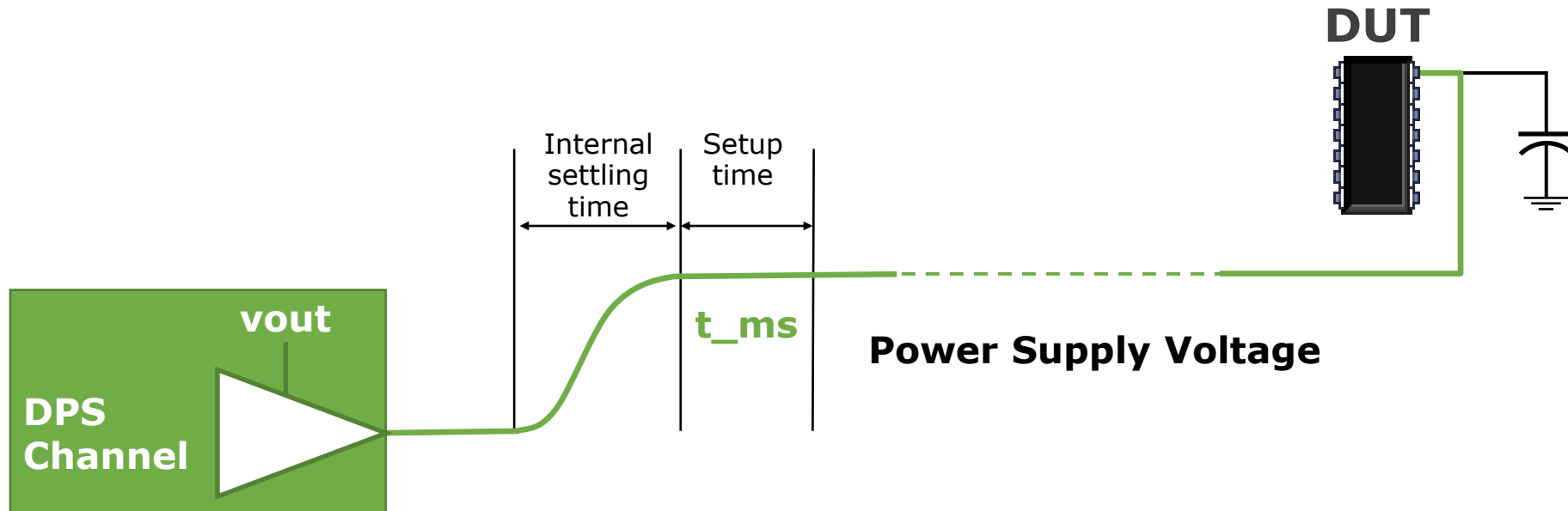


Parametric Measurement Unit

2 modes of operation

- Current generator & **Voltage Meas** ①
- Voltage generator & **Current Meas** ②

DEVICE POWER SUPPLY (DPS)

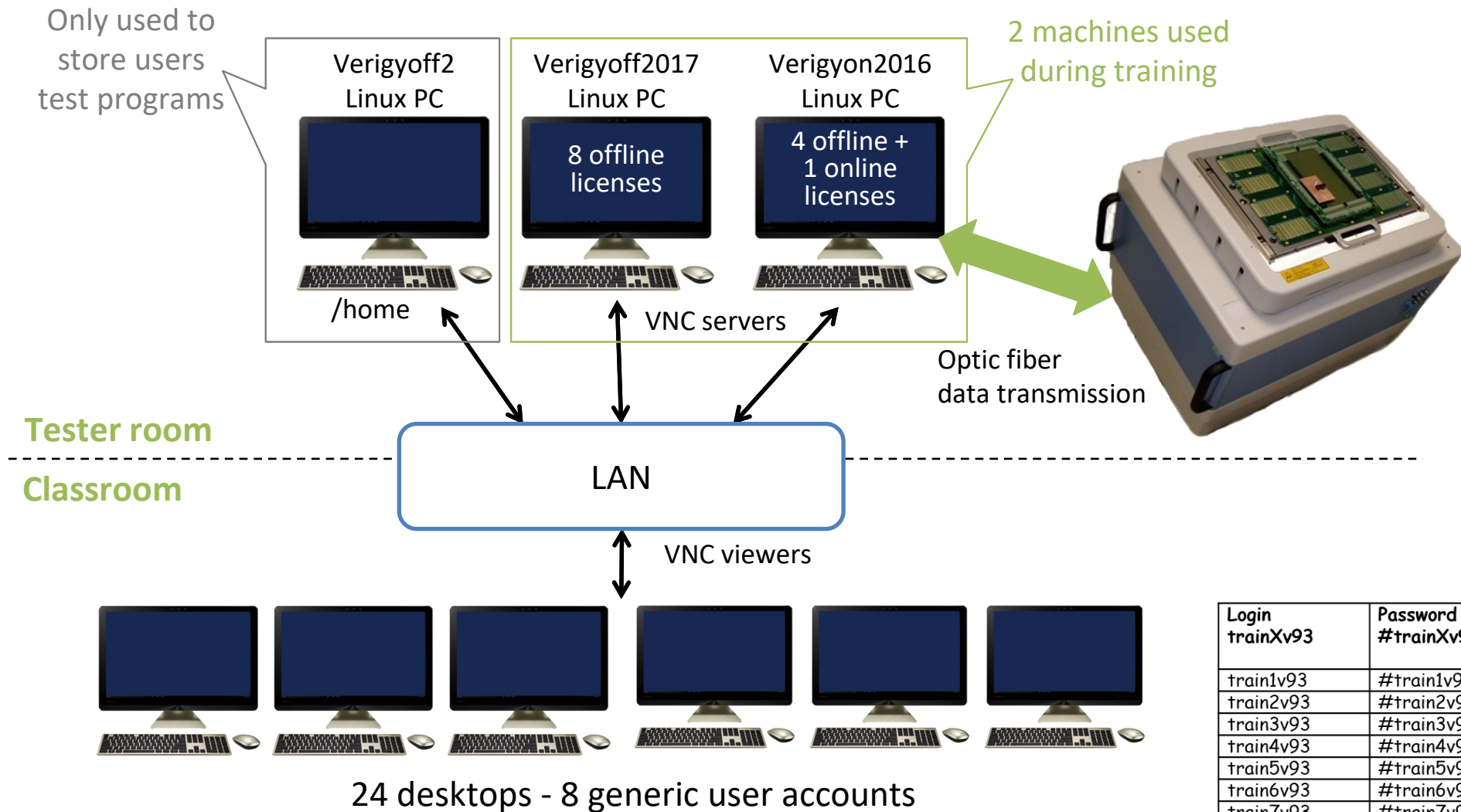


DPS parameters

- **vout** (V) power supply voltage
- **t_ms** (ns) setup time
- **ilimit** (A) connect current limit (to prevent destruction of the DUT)

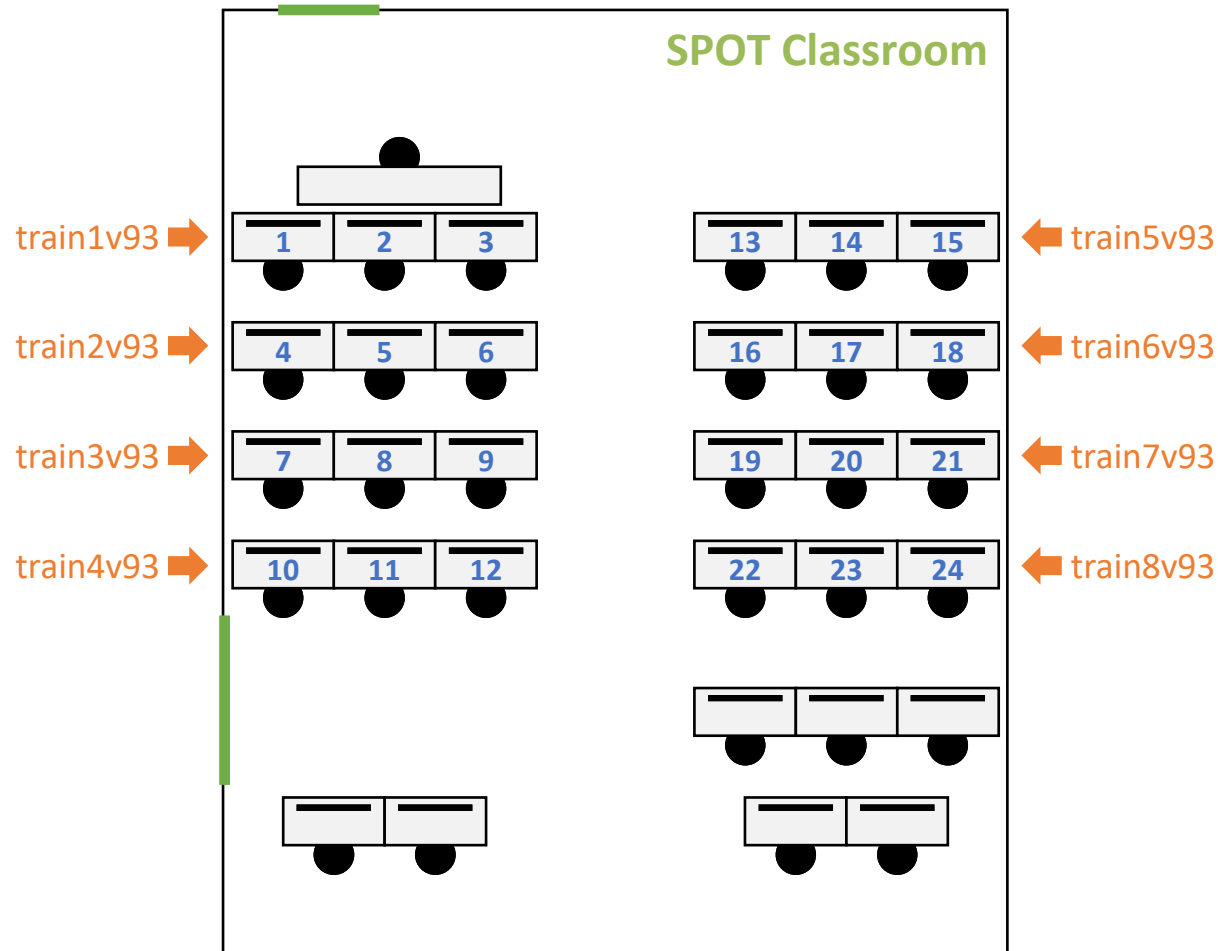


LAB ENVIRONMENT



Login	Password	Y: VNC display number
trainXv93	#trainXv93#	
train1v93	#train1v93#	71
train2v93	#train2v93#	72
train3v93	#train3v93#	73
train4v93	#train4v93#	74
train5v93	#train5v93#	75
train6v93	#train6v93#	76
train7v93	#train7v93#	77
train8v93	#train8v93#	78

LAB ENVIRONMENT



Tester connection

Only 8 offline licenses run at the same time during practice (memory issues)

- 2 on verigyon2016
- 6 on verigyoff2017

Work in "trio"

Login trainXv93	Password #trainXv93#	Y: VNC display number	M: Default machine for offline connection
train1v93	#train1v93#	71	verigyon2016
train2v93	#train2v93#	72	verigyon2016
train3v93	#train3v93#	73	verigyoff2017
train4v93	#train4v93#	74	verigyoff2017
train5v93	#train5v93#	75	verigyoff2017
train6v93	#train6v93#	76	verigyoff2017
train7v93	#train7v93#	77	verigyoff2017
train8v93	#train8v93#	78	verigyoff2017

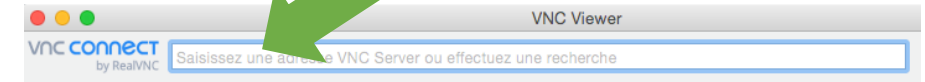
Local PC connection

- Login: etudiant
- Password: &tudiant

LAB ENVIRONMENT

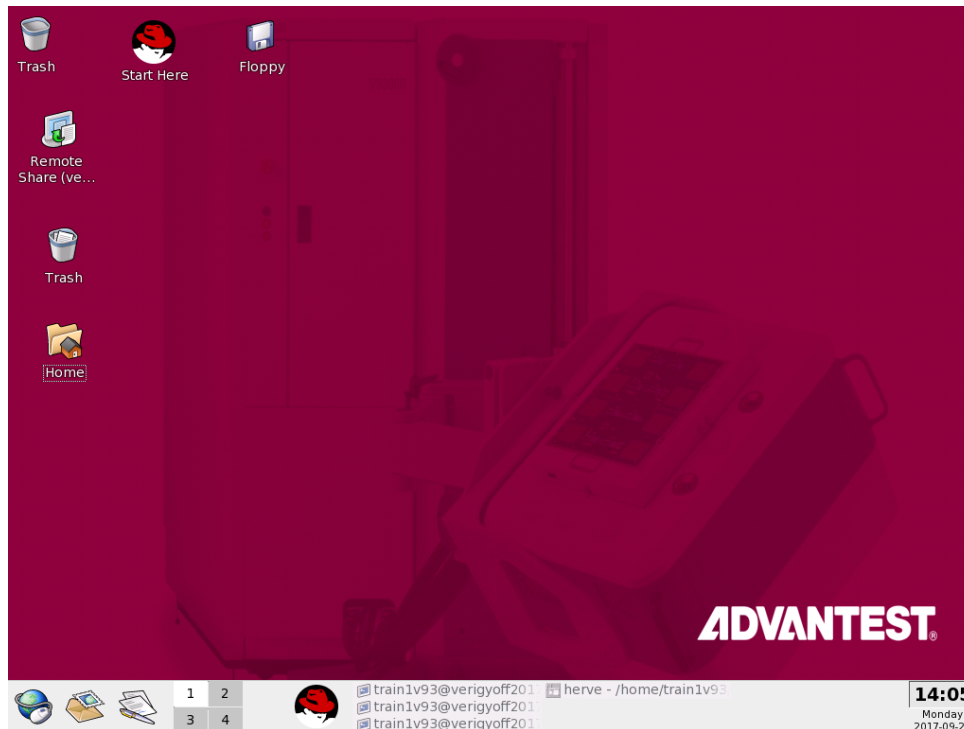
- Procedure to start Graphical Interface of tester SW

1/ Connect to a **verigy** machine using **VNC**

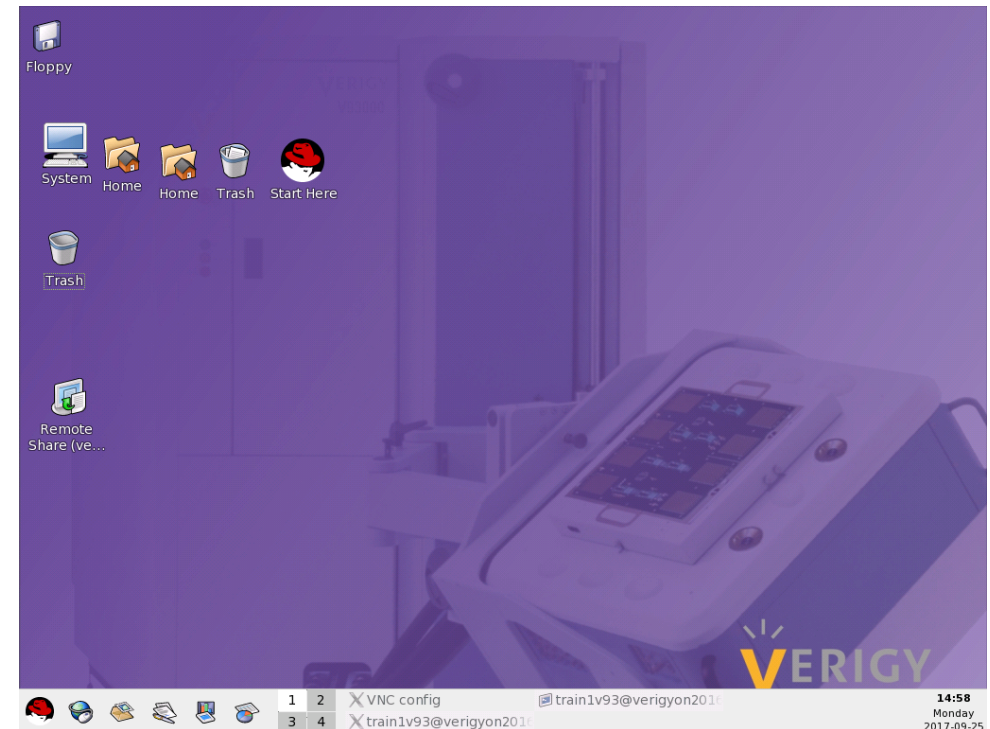


M.cnfm.fr:Y

Screen of verigyoff2017



Screen of verigyon2016

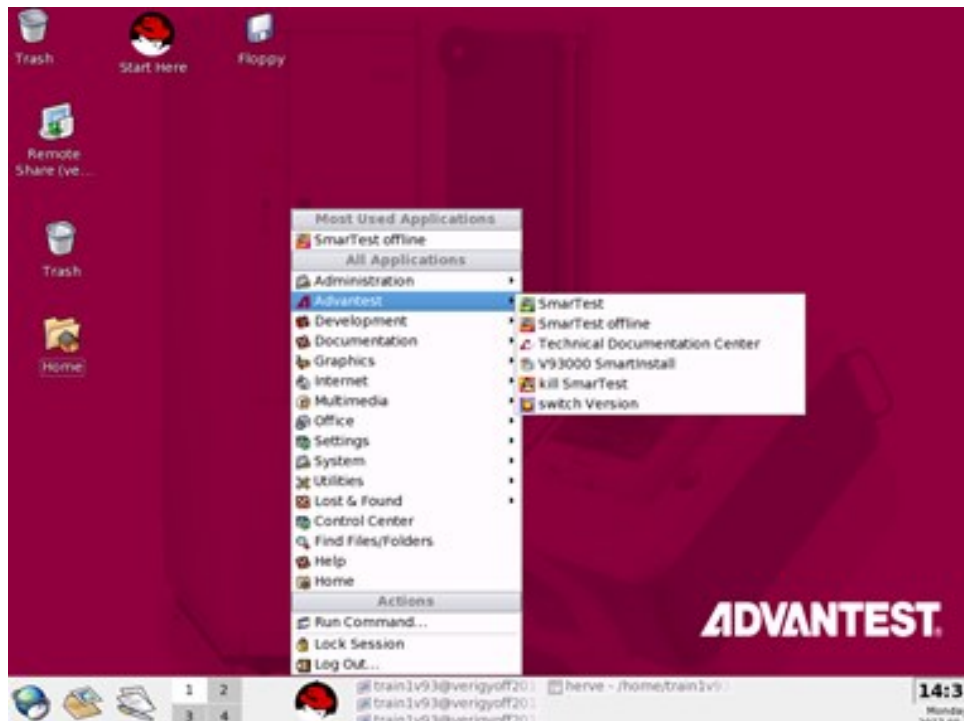


LAB ENVIRONMENT

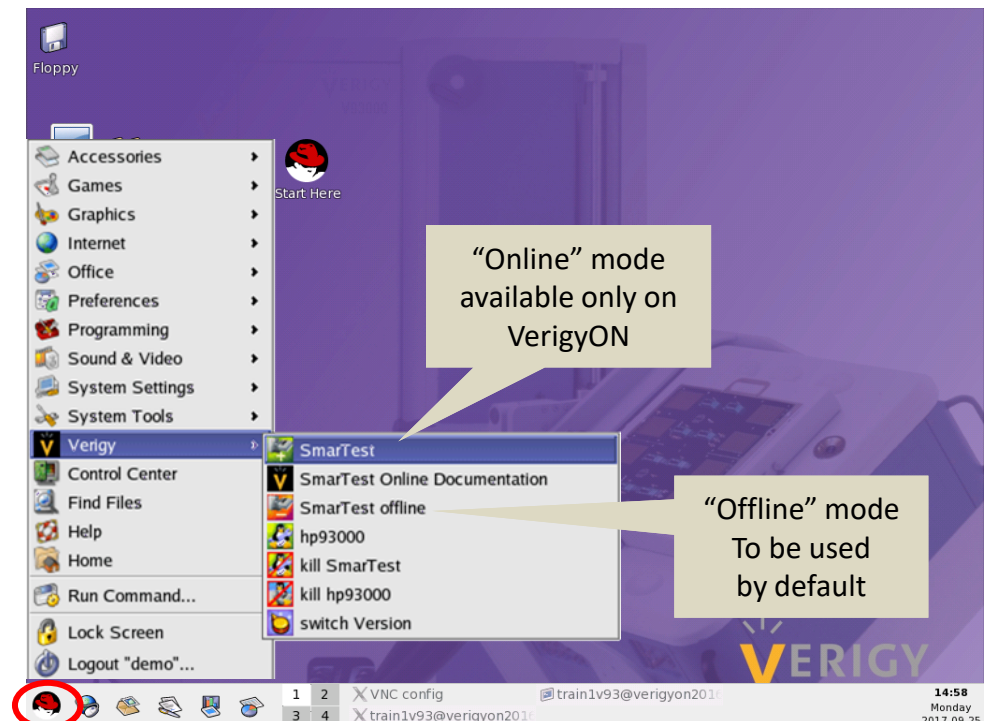
- Procedure to start Graphical Interface of tester SW

2/ Launch **SmarTest** from the start menu “” (“RedHat” menu)

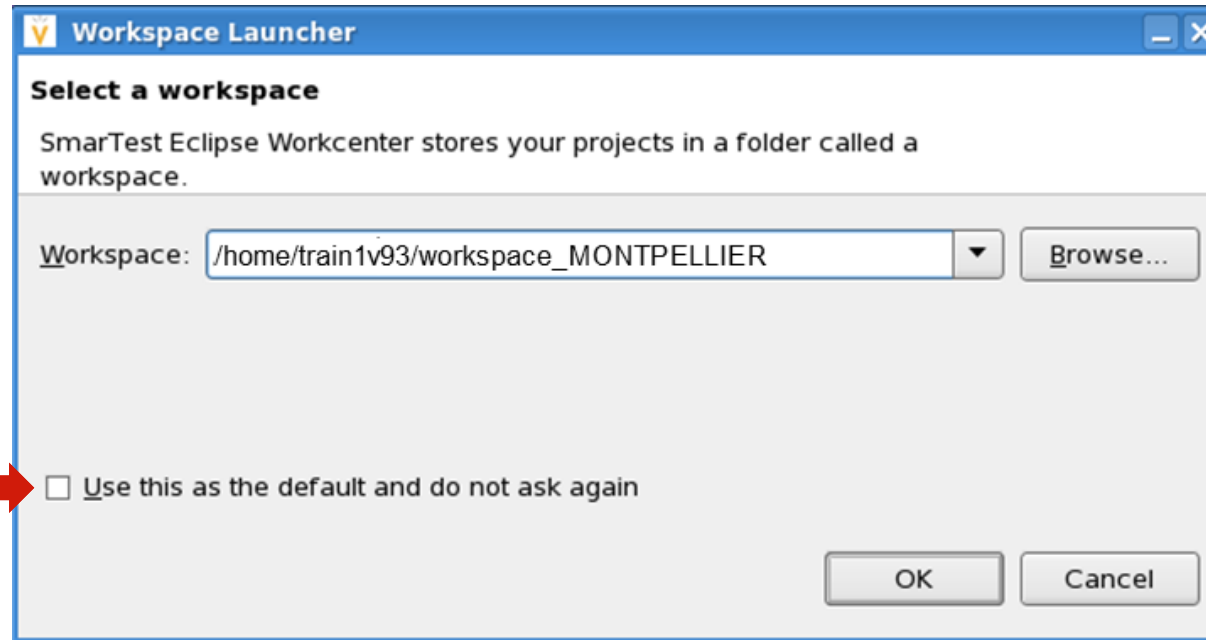
verigyoff2017



verigyon2016



AT STARTUP: WORKSPACE SELECTION



**NEVER SELECT
THIS OPTION**

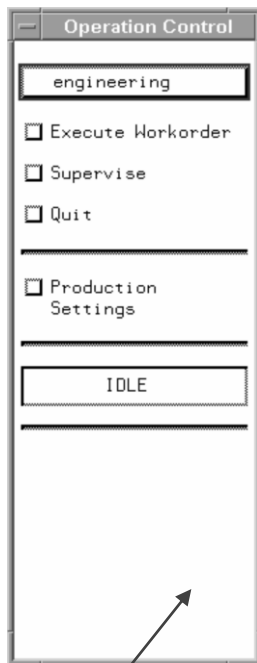


Workspace stores users' interface configuration
Do not mix it with test program explorer path

AT STARTUP: 3 WINDOWS

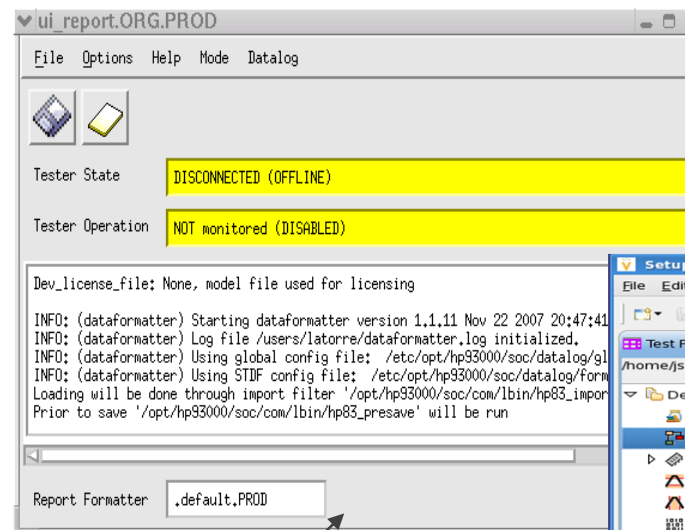
“SmarTest Eclipse Workcenter”

- **MAIN WINDOW**
- Provide all tools to:
 - Create & load configuration files
 - Create & execute a test flow
 - ...



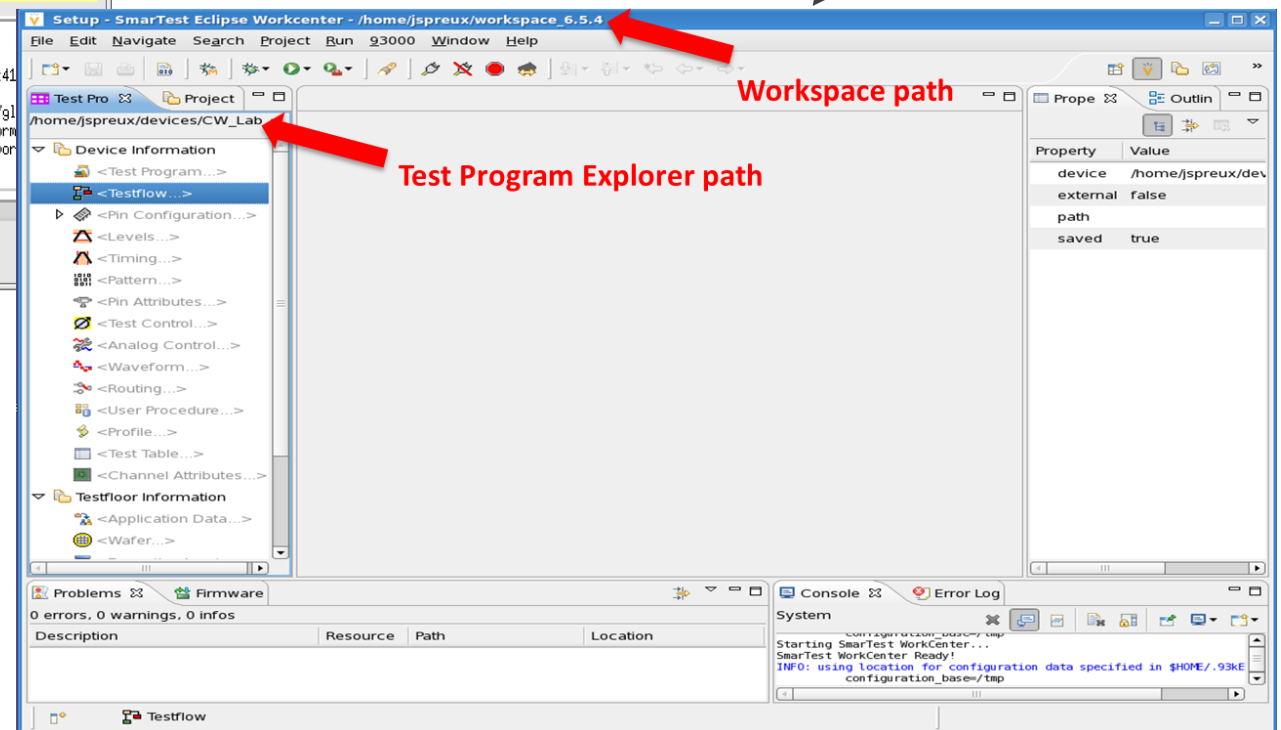
“Operation Control”

- Tasks execution
- Datalog Formatting

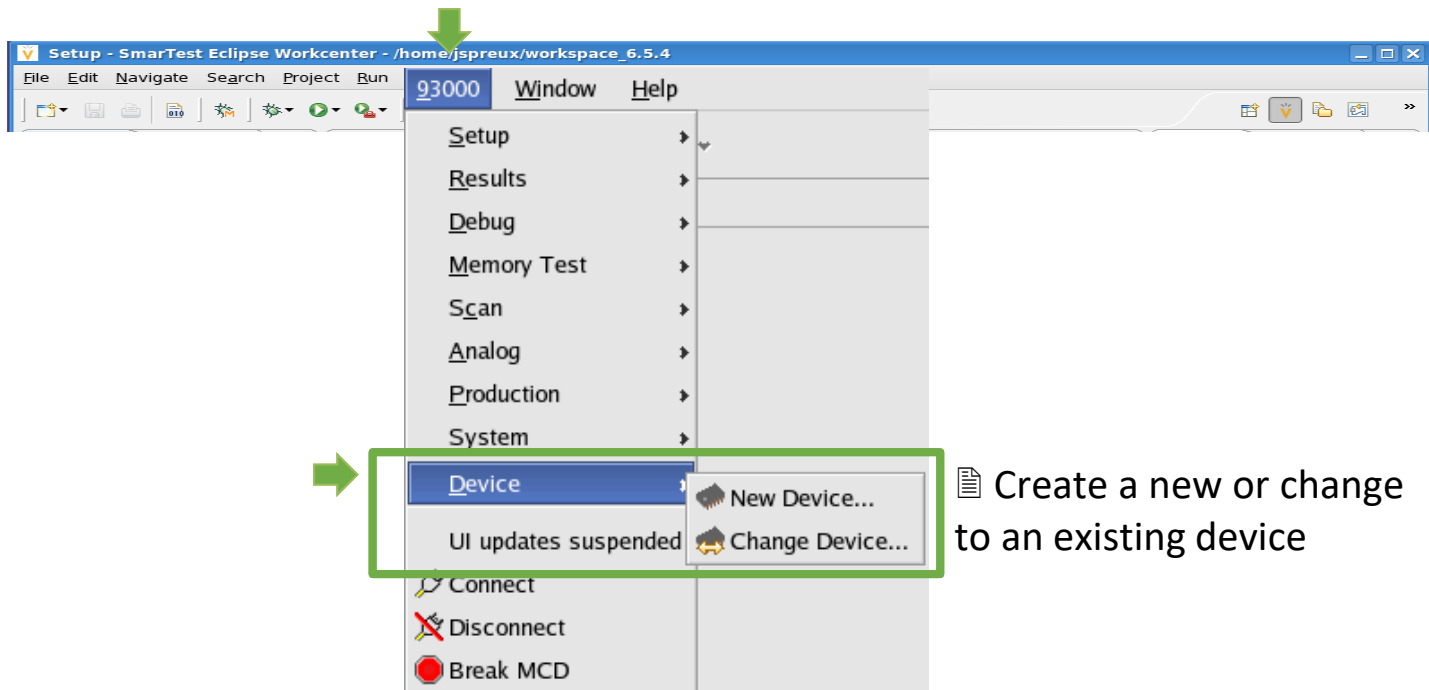


“ui_report”

- Syntax errors
- Test execution issues
- Test results



FIRST STEP: CREATE A DEVICE



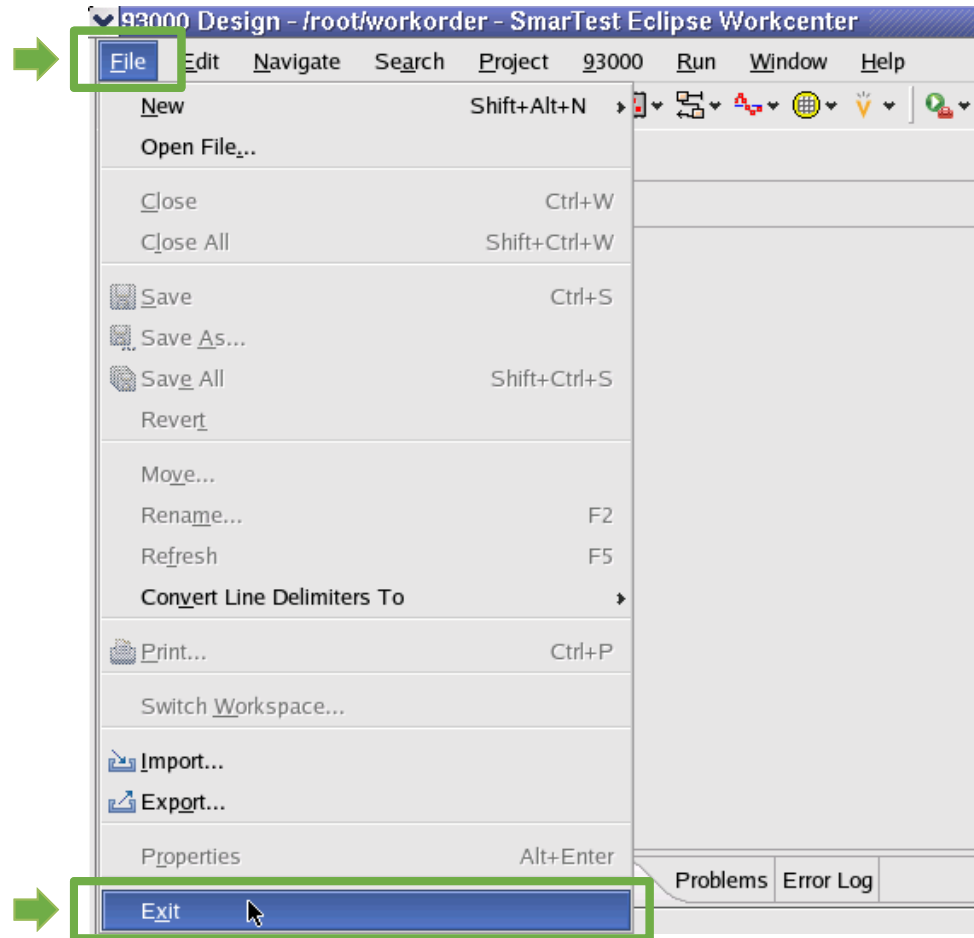
- To create a device, click
93000 > Device > New Device

- Device creation will automatically generate all sub-directories necessary to develop & store the test program specific to this device



```
[root@localhost training]# ls -a
.          ch_attributes  license      scan        testprog
..         configuration lock_file    scan_res    timing
.technology data_set        ment_llapg   scrambling   timing_dgrm
analog_control di_report      ment_patterns shmoo        vectors
applicat   error_map      ment_repair  state_list   wafertyp
bitmap     fail_memory    pin_attributes testflow     waste
bitmap_conf format          report       testflow_vee waveform
calibration levels         routing      testfunc
```

EXITING SMARTEST

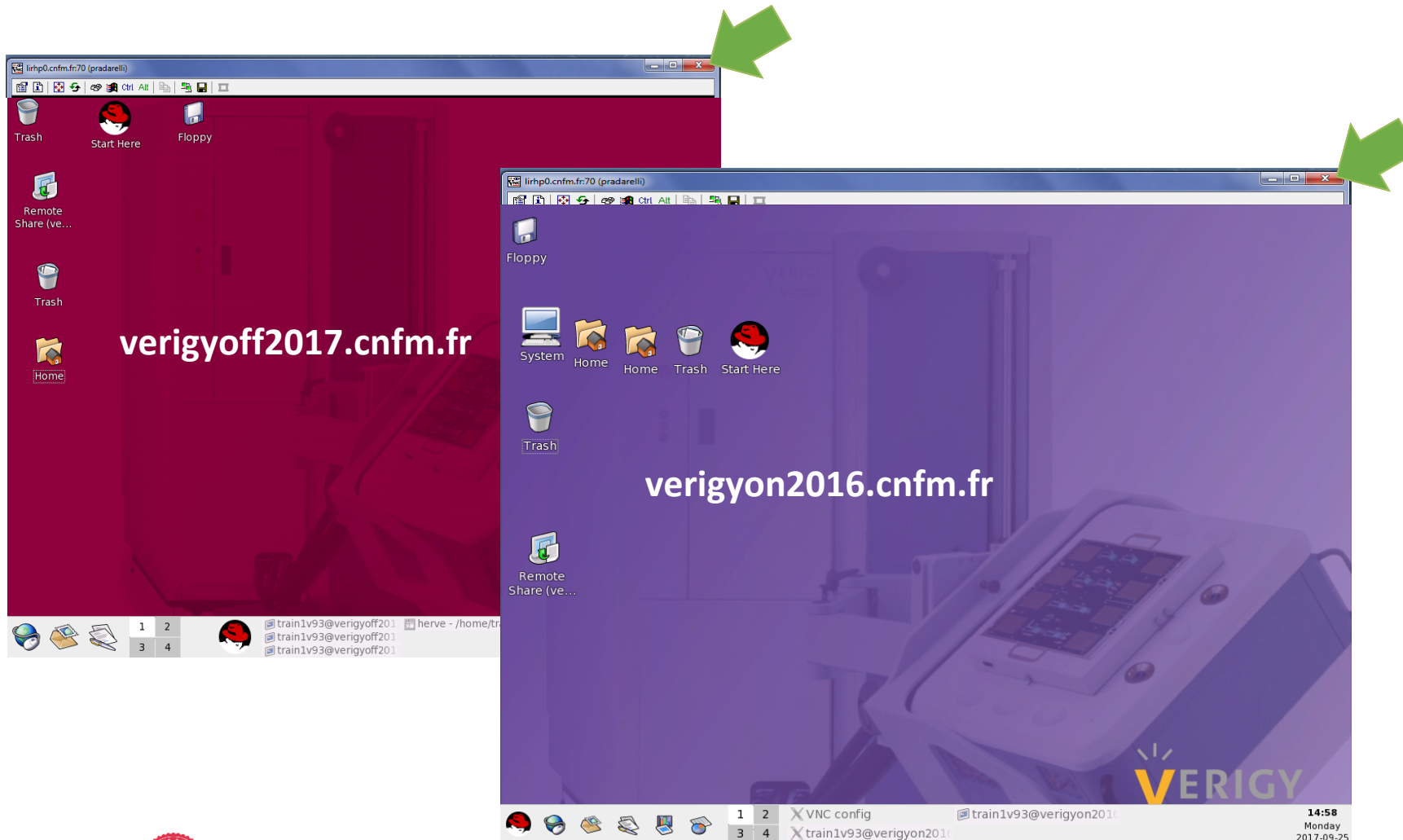


- To exit SmarTest, click **File > Exit**

To kill the entire SmarTest process, type the following command in a Terminal window:

```
/opt/hp93000/soc/prod_env/sbin/kill_smarTest
```

EXITING VNC



- Close the window to exit VNC



DO NOT LOGOUT!
=> VNC server must be launched again



Lab:



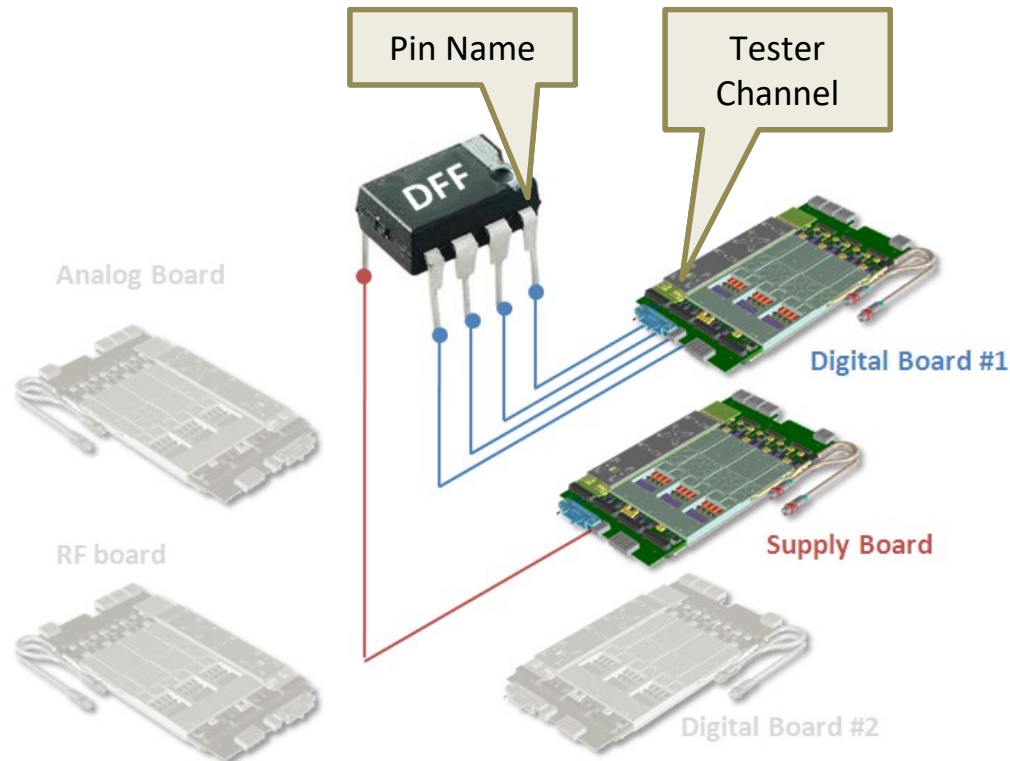
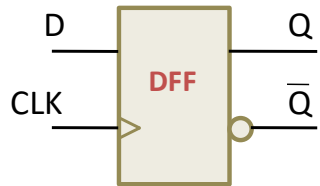
First Steps with SmarTest - Part 1



PINS

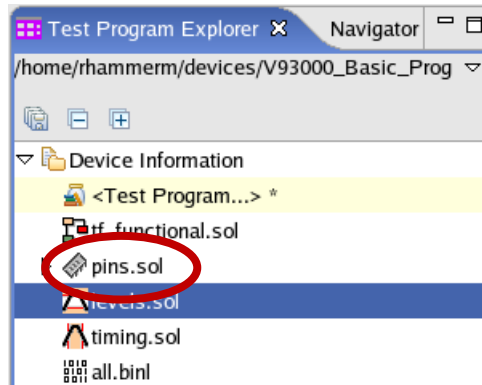
- First element to be defined
 - Link between **Pin Names** and **Tester Channels**
 - Definition of **Pin Type**

EXAMPLE



Pin Name	Pin Type	Tester Channel
CLK	Input	10101
D	Input	10102
Q	Output	10103
$\bar{Q}$	Output	10104
V _{CC}	Supply	10201

PIN SETTING IN SMARTTEST



All following definitions
(levels, timing, pattern)
will be made using Pin Name

From Datasheet

From DIB

Pin Setting

Site : 1 Of 1

CONTEXT: DEFAULT

	Pin No	Pin Name	Mode	Type	DUT Board	Tester Channel
1	12	CP	std	i	0.0	10102
2	11	DS0	std	i	0.0	10101
3	18	DS7	std	i	0.0	10108
4	7	I/O0	std	io	0.0	10114
5	13	I/O1	std	io	0.0	10103
6	6	I/O2	std	io	0.0	10113
7	14	I/O3	std	io	0.0	10104
8	5	I/O4	std	io	0.0	10112
9	15	I/O5	std	io	0.0	10105
10	4	I/O6	std	io	0.0	10111
11	16	I/O7	std	io	0.0	10106
12	8	Q0	std	o	0.0	10115
13	17	Q7	std	o	0.0	10107
14	1	S0	std	i	0.0	10110
15	19	S1	std	i	0.0	10109
16		Vcc		DPS+	0.0	DPS11
17	9	_MR	std	i	0.0	10116

Pin Type determines
the parameters that
will be defined

PIN SETTING IN SMARTTEST

Test Program Explorer

/usr/project/74ACT299

pins

Pin Setting

Groups

- all_in
- all_out
- ctrl
- io_in
- io_out
- io_pins
- mode
- ser_in
- ser_out

Ports

- Core Allocation
- DPS Channel Mode
- Utility Purpose

Open

- Add Context...
- Delete Context...
- Define Site...
- Apply

*Pin Setting

Site : 1 Of 1

CONTEXT: DEFAULT

	Pin No	Pin Name	Mode	Type	DUT Board	Tester Channel
1	12	CP	std	i	0.0	10102
2	18	DS7	std	i	0.0	10108
3		DS0	std	i	0.0	10101
4	19	S1	std	i	0.0	10109
5	1	S0	std	i	0.0	10110
6	9	_MR	std	i	0.0	10116
7	17	Q7	std	o	0.0	10107
8	8	Q0	std	o	0.0	10115
9	16	I/O7	std	io	0.0	10106
10	4	I/O6	std	io	0.0	10111
11	15	I/O5	std	io	0.0	10105
12	5	I/O4	std	io	0.0	10112

Error message if:

- test channel already used
- test channel unavailable

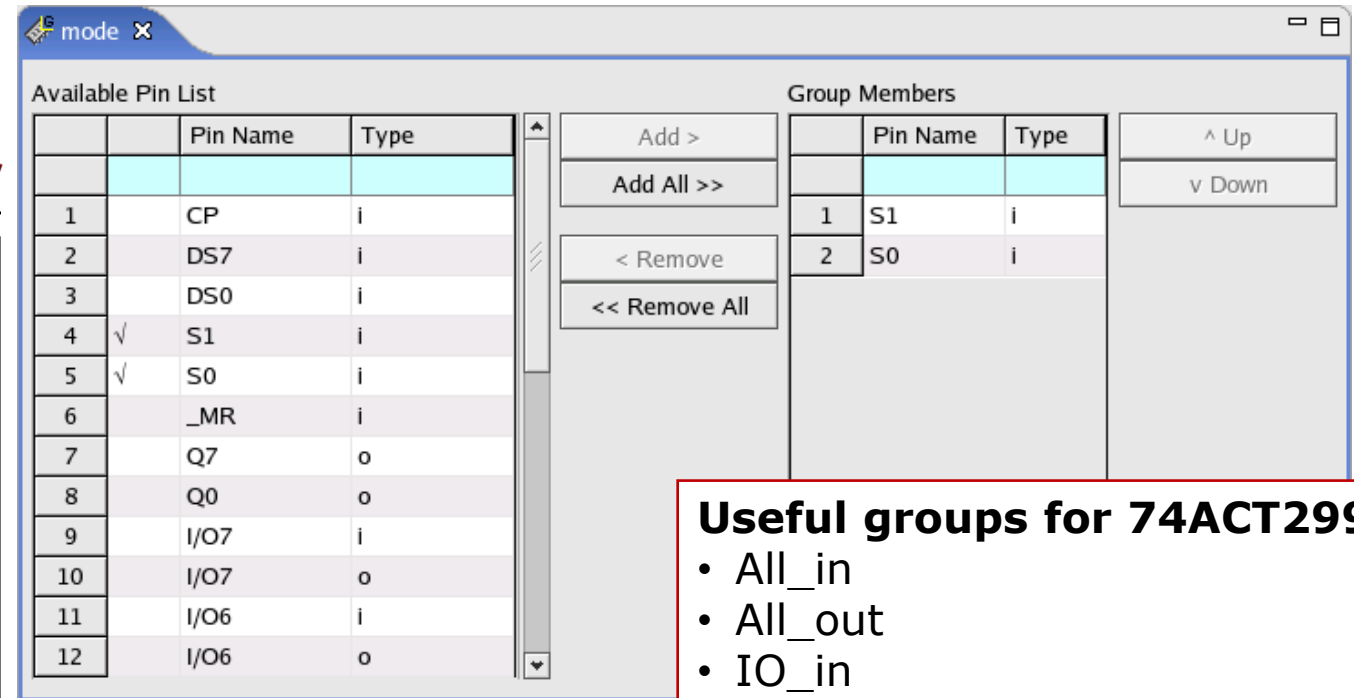
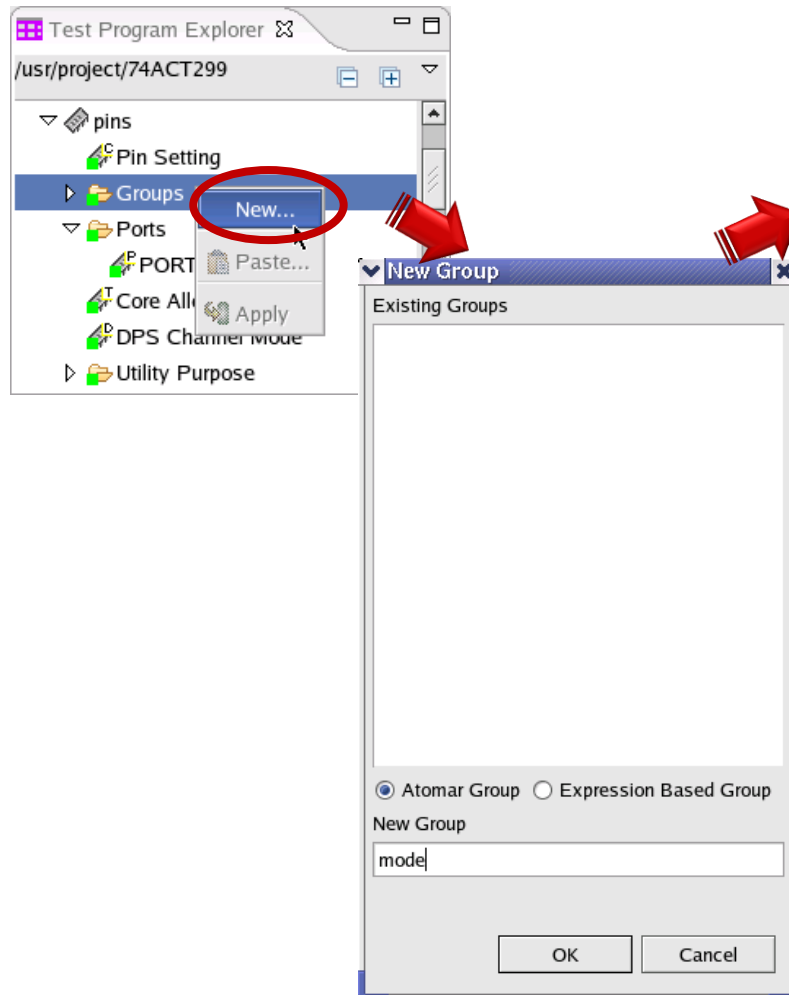


No error message if:

- test channel exists, even if the DUT pin is not connected to this channel

PIN SETTING IN SMARTTEST

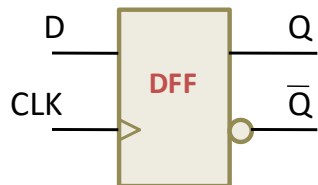
Defining Groups



Useful groups for 74ACT299

- All_in
- All_out
- IO_in
- IO_out
- IO_pins
- Mode
- Ser_in
- Ser_out

EXAMPLE



LEVELS

Relaxed Levels

	Vil	Vih
D, CLK	0V	Vcc
	Vol	Voh
Q, Qb	$V_{cc}/2 - 10\% V_{cc}$	$V_{cc}/2 + 10\% V_{cc}$

Equation Set

Supply pins

EQNSET 1 "Without specs & eqn"

DPSPINS Vcc

vout = 5.0

Level Set

Input pins

LEVEL SET 1 "The only level set"

PINS D, CLK

vil = 0

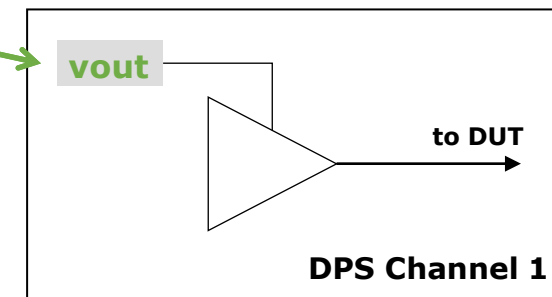
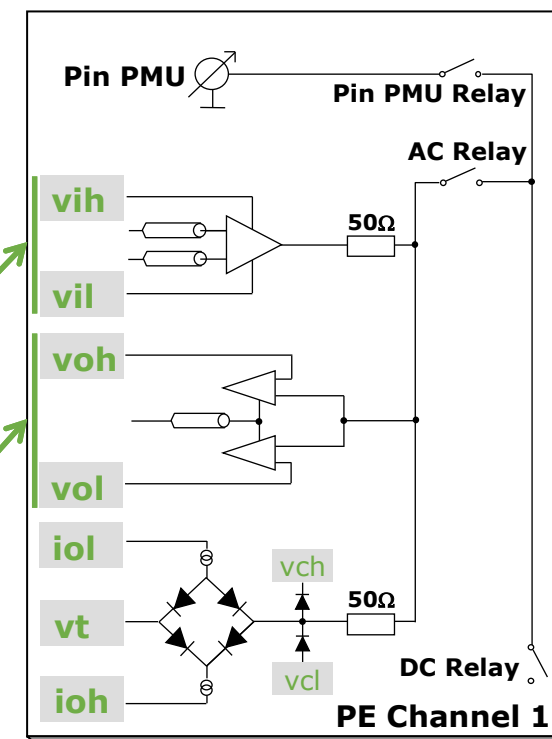
vih = 5.0

Output pins

PINS Q Qb

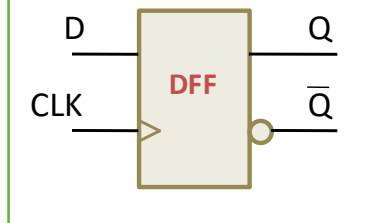
vol = 2.25

voh = 2.75



LEVELS

EXAMPLE



VCC: Spec variable

Relaxed Levels

	Vil	Vih
D, CLK	0V	Vcc
	Vol	Voh
Q, Qb	$V_{cc}/2 - 10\% V_{cc}$	$V_{cc}/2 + 10\% V_{cc}$

Equation Set

Supply pins

Level Set

Input pins

Output pins

EQNSET 1 "Without specs & eqn"

DPSPINS Vcc

vout = 5.0

LEVEL SET 1 "The only level set"

PINS D, CLK

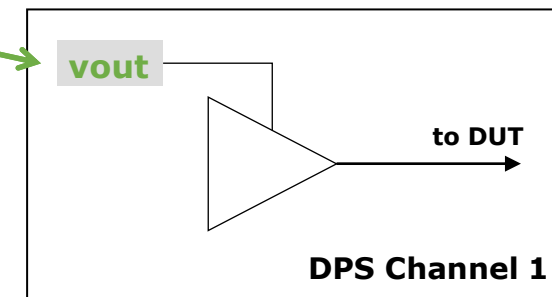
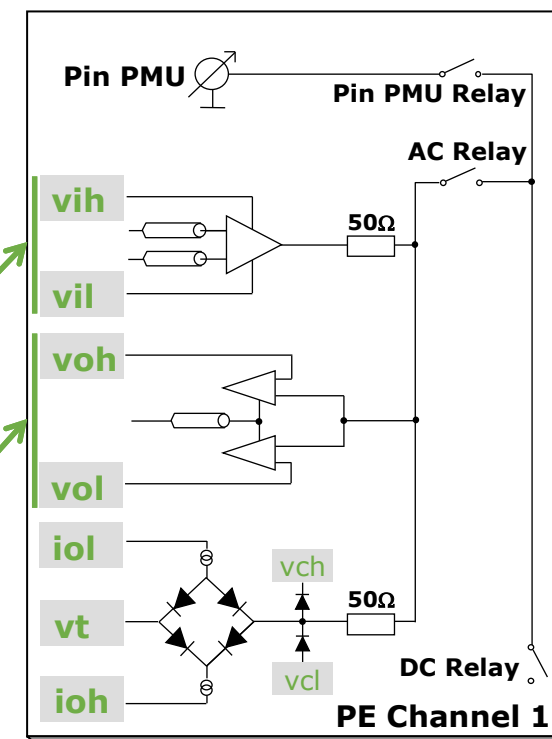
vil = 0

vih = 5.0

PINS Q Qb

vol = 2.25

voh = 2.75



EQNSET 1 "With specs & eqn"

DPSPINS Vcc

vout = VCC

LEVEL SET 1 "The only level set"

PINS D, CLK

vil = 0

vih = VCC

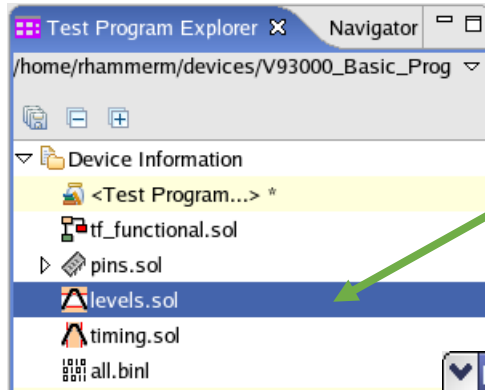
PINS Q Qb

vol = $V_{CC}/2 - 0.1 \times V_{CC}$

voh = $V_{CC}/2 + 0.1 \times V_{CC}$

In the Test Program Explorer

1. Load levels file
2. Open or Double-click on the levels item



2. Open or Double-click on the levels item



Switch between I/O pins & DPS pins

Open EQN SET Editor

The screenshot shows the "Level Setup" dialog box with the "Select" menu open. The menu options are:

- I/O pins
- DPS pins
- DPS overvoltage
- Show I/O Eqn. & Specs Results
- Show FAST Eqn. & Specs Results
- Show DPS Eqn. & Specs Results
- Select Specification...
- Edit Specifications
- Edit Equations

A red arrow points to the "I/O pins" option. The background window displays a table with columns for termination and clamp parameters.

LEVEL SETTING IN SMARTTEST

LEVEL EQUATION SET EDITOR

```
/var/opt/hp93000/soc/tmp/93k.4GWsYU/edit_lvleqn
File Edit Search Preferences Shell Macro Windows Help
pt/hp93000/soc/tmp/93k.4GWsYU/edit_lvleqn byte 159 of 290 L: 18 C: 20

1 EQNSET 1 "gross"
2
3 SPECS
4 VCC [V]
5 VIH [V]
6 VIL [V]
7 VOH [V]
8 VOL [V]
9
10
11 DSPINS Vcc
12 vout = 0
13 ilimit = 1000
14 t_ms = 4
15 offcurr= act
16
17
18 LEVELSET 1 "nominal"
19
20 PINS ctrl ser_in
21 vil= VIL
22 vih= VIH
23
24 PINS ser_out
25 vol= VOL
26 voh= VOH
27
28 PINS io_pins
29 vil= VIL + 0.1
30 vih= VIH + 0.1
31 vol= VOL
32 voh= VOH
33
```

Several EQNSETs can exist

Values are assigned to Spec variables in the Spec Tool

Several LEVELSETs can exist

Possible to use pin-group names

Values can be expressed with variables

LEVEL SETTING IN SMARTTEST

```
1 EQNSET 1 "gross"
2
3 SPECS
4 VCC [V]
5 VIH [V]
6 VIL [V]
7 VOH [V]
8 VOL [V]
9
10
11 DPSPINS Vcc
12 vout = 0
13 ilimit = 1000
14 t_ms = 4
15 offcurr= act
16
17
18 LEVELSET 1 "non
19
20 PINS ctrl ser_
21 vil= VIL
22 vih= VIH
23
24 PINS ser_out
25 vol= VOL
26 voh= VOH
27
28 PINS io_pins
29 vil= VIL + 0.1
30 vih= VIH + 0.1
31 vol= VOL
32 voh= VOH
33
```



Click on **Download** icon to update the actual settings in the ATE

SpecTool

File Select Change Edit Sort Display Doc Help

Levels (modified, download required)

Specification 1 1 gross_levels

Equation 1

Name	Actual	Minimum	Maximum	Measured	Unit	Comment
VIH	2.8				V	
VIL	2.2				V	
VOH	2.4				V	
VOL	0.4				V	
VCC	5				V	

Enter Values

LEVEL
SPEC TOOL

LEVEL SETTING IN SMARTTEST



Define a format to display pin groups
instead of all individual pins

ACTUAL
SETTINGS

"Show I/O Eqn.
& Specs Results"

Level Setup

Select Edit Doc Format standard

Eqn# Sps# Lset# of 3 Level

Specification Equation

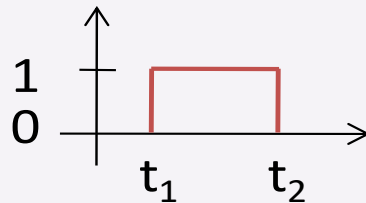
pin/group name	pin type	level[V]		mode	termination				swing	offset	clamp		
		low	high		lev[V]	lol[mA]	loh[mA]				mode	low[V]	high[V]
CP	i	0.000	4.250	off							off	-2.000	7.000
mode	i	0.000	4.250	off							off	-2.000	7.000
ser_in	i	0.000	4.250	off							off	-2.000	7.000
io_in	i	0.000	4.250										
io_out	o	2.200	2.300	off							off	-2.000	7.000
ser_out	o	2.200	2.300	off							off	-2.000	7.000

TIMING

- Concept

- Define waveforms by associating actions to edges ➡ **Waveform Tables**
- Specify tester period and position of edges ➡ **Timing Sets**

Waveform Tables



Timing Sets

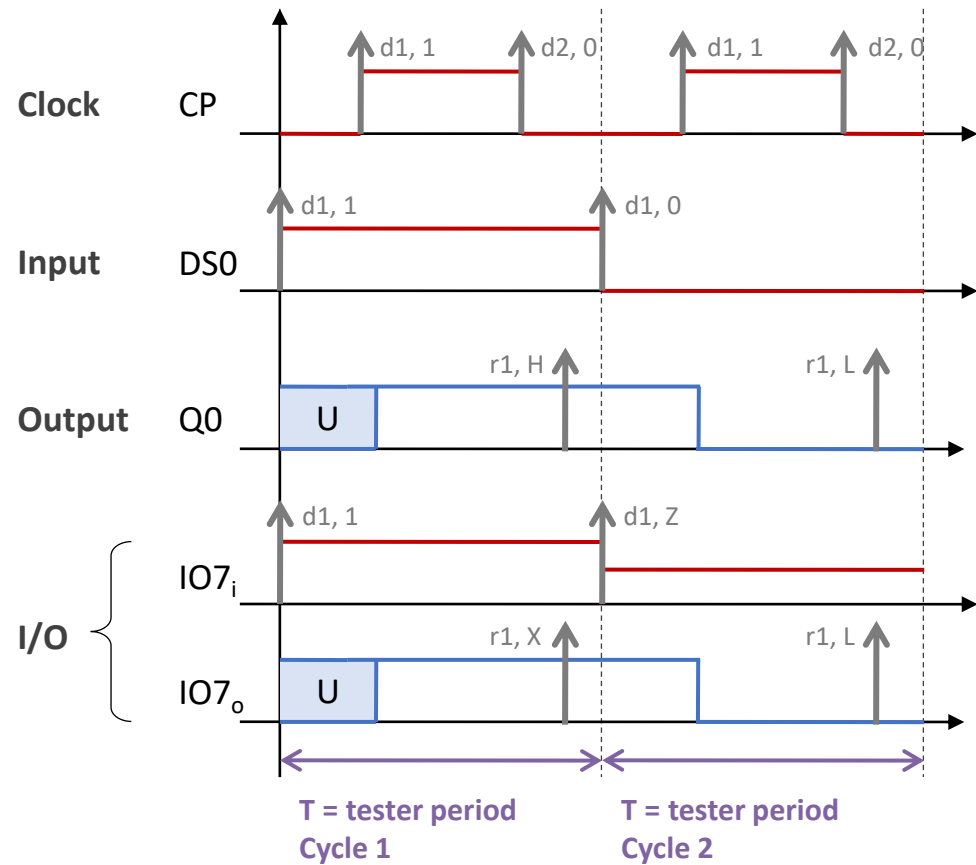
Tester timing resources per pin

- Input pins: 8 drive edges (d1, d2, ..., d8)
- Output pins: 8 receive edges (r1, r2, ..., r8)
- I/O pins: 8 drive edges + 8 receive edges

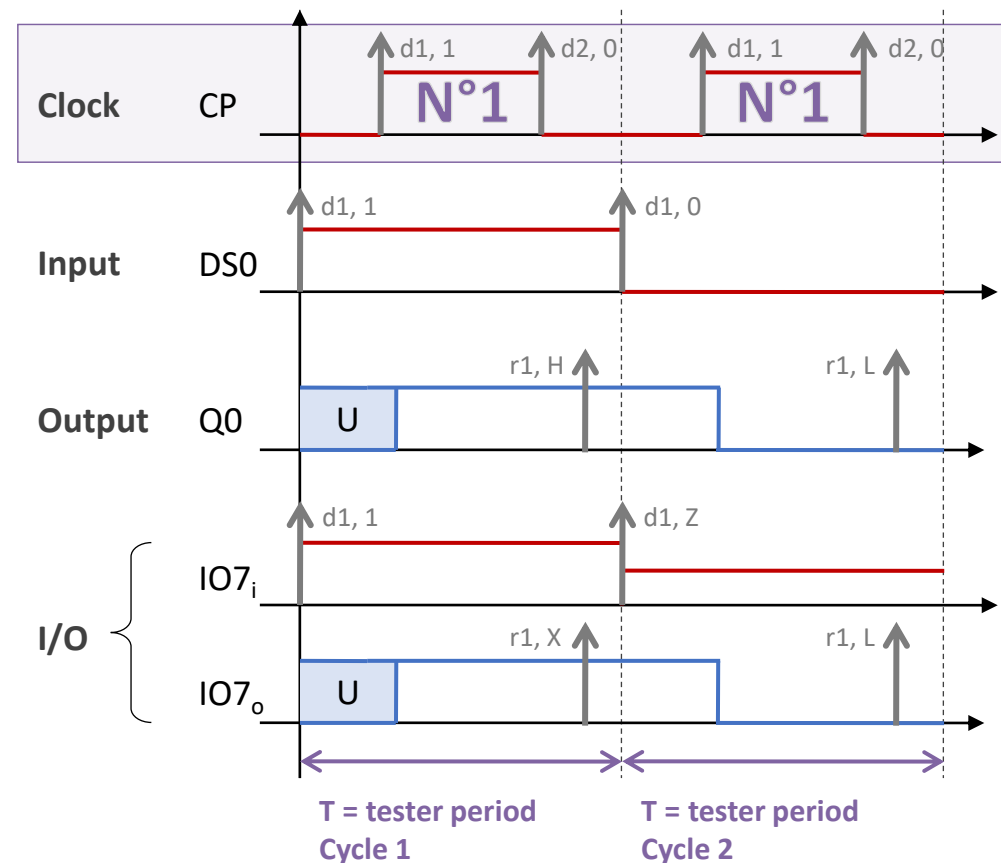
Actions

- Drive actions
 - 0: Drive '0'
 - 1: Drive '1'
 - Z: High impedance
 - N: No action
- Receive actions (*edges*)
 - L: Compare to 'Low'
 - H: Compare to 'High'
 - M: Compare to 'Intermediate'
 - X: Don't care

TIMING PROGRAMMING



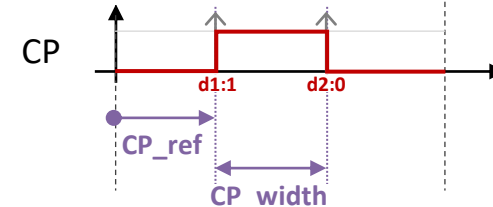
TIMING PROGRAMMING



CP Waveform N° 0



CP Waveform N° 1



Programming – Clock

Waveforms

N° 0 - d1:0 d2:0 (*Clock Inactive*)

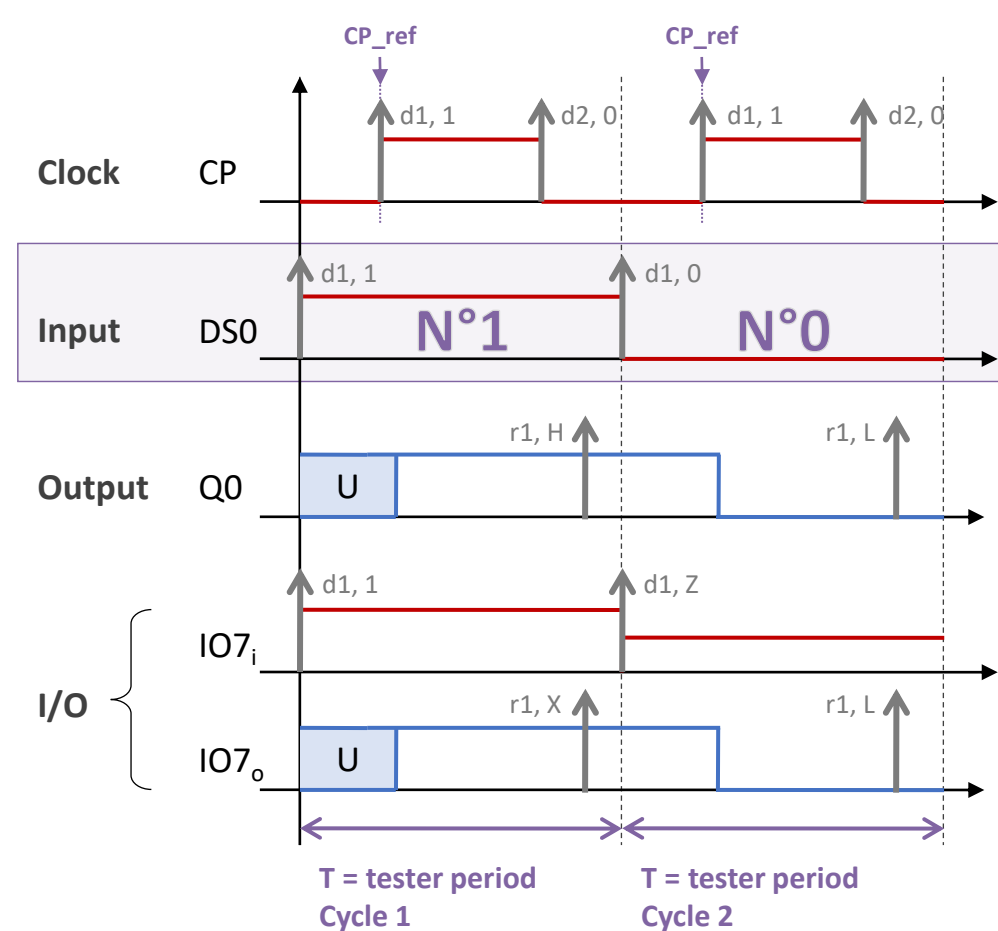
N° 1 - d1:1 d2:0

Edges Position

d1: CP_ref

d2: CP_ref + CP_width or after

TIMING PROGRAMMING



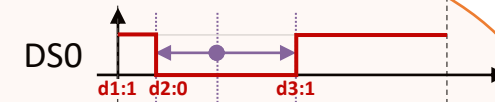
DS0 Waveform N° 0



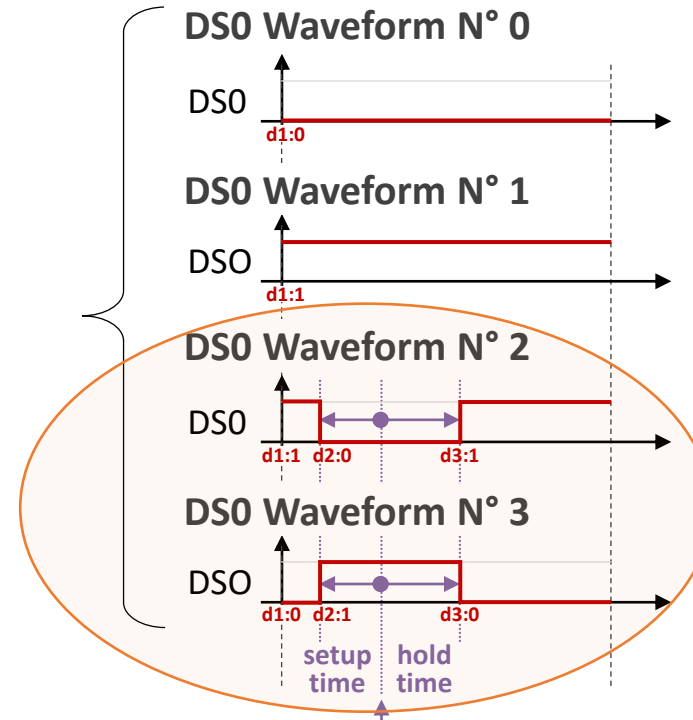
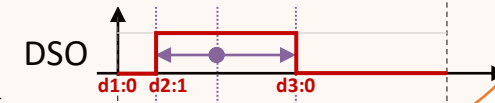
DS0 Waveform N° 1



DS0 Waveform N° 2



DS0 Waveform N° 3



Programming – Input

Waveforms

- N° 0 - $d1:0$
 - N° 1 - $d1:1$
 - N° 2 - $d1:1$ $d2:0$ $d3:1$
 - N° 3 - $d1:0$ $d2:1$ $d3:0$
- DNRZ format* (for N° 0 and N° 1)
SBC format (for N° 2 and N° 3)

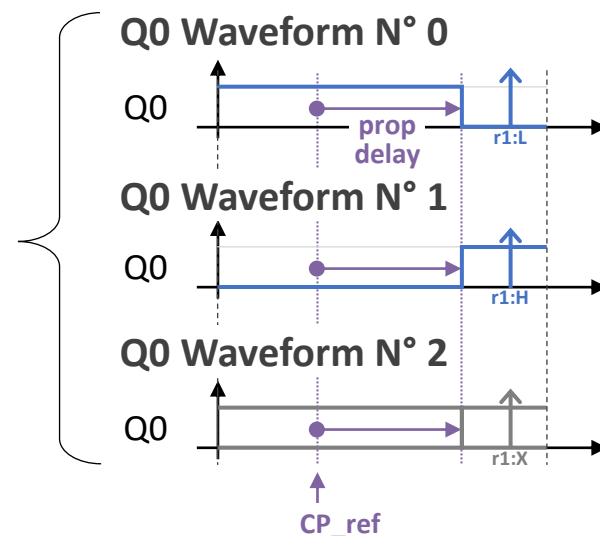
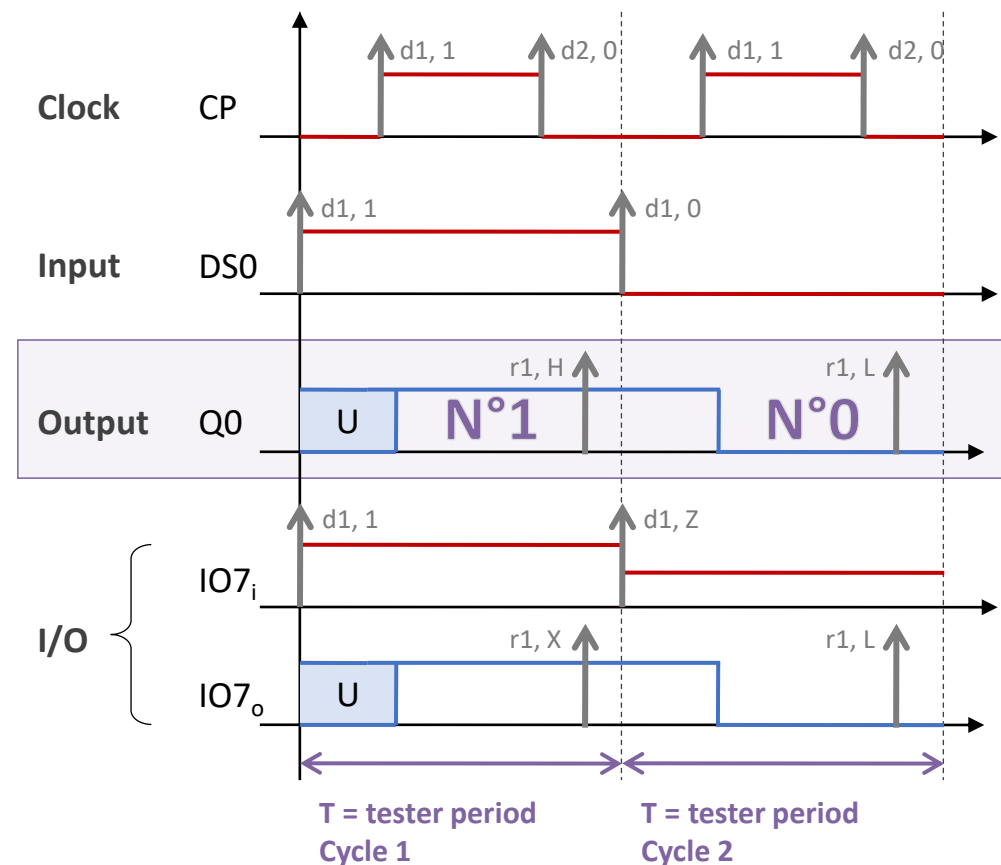
Edges Position

- $d1$: 0ns
- $d2$: CP_{ref} - setup_time or before
- $d3$: CP_{ref} + hold_time or after

WF definition to handle verification of setup & hold times:

- SBC format (3 edges)

TIMING PROGRAMMING



Programming – Output

Waveforms

N° 0 - $r1:L$

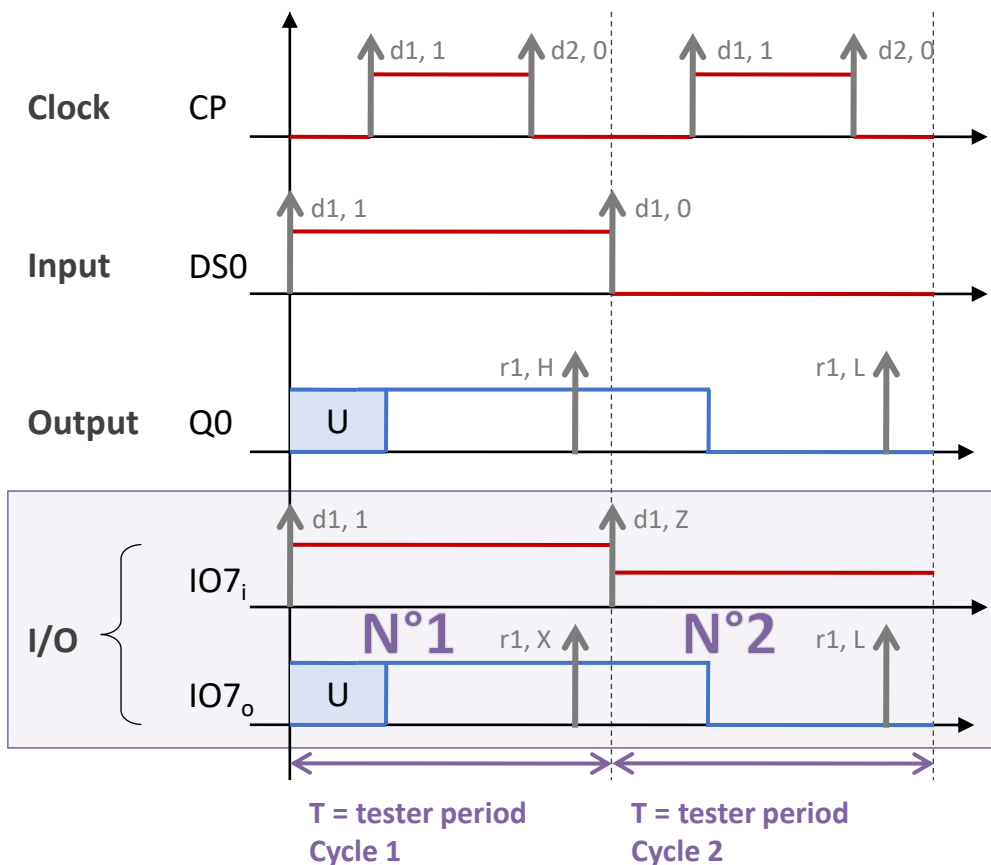
N° 1 - $r1:H$

N° 2 - $r1:X$

Edges Position

$r1$: $CP_ref + prop_delay$ or after

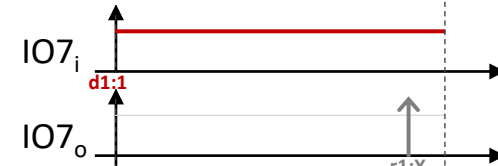
TIMING PROGRAMMING



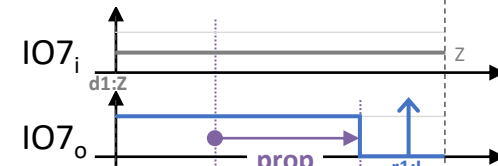
IO7 Waveform N° 0



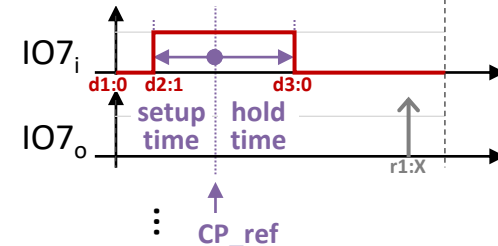
IO7 Waveform N° 1



IO7 Waveform N° 2



IO7 Waveform N° 5



Programming – I/O Pins

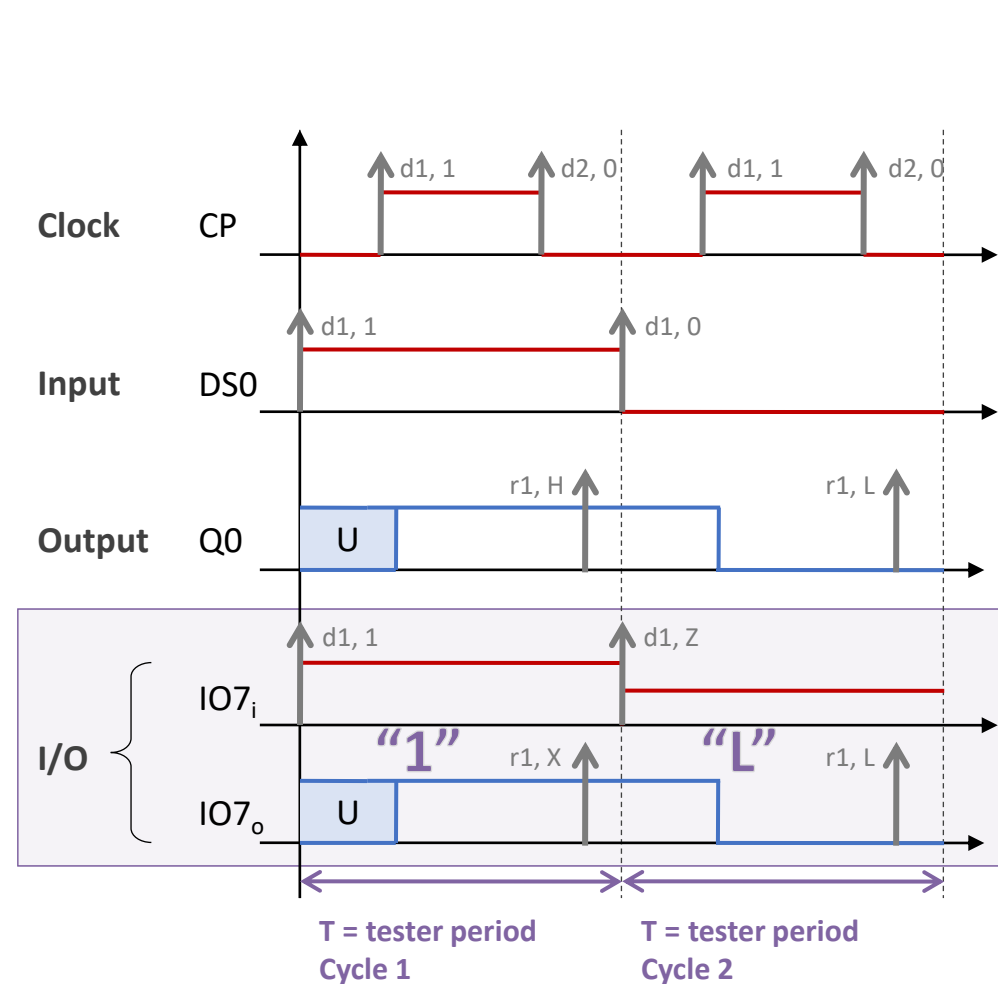
Waveforms

- N° 0 - $d1:0$ $r1:X$
- N° 1 - $d1:1$ $r1:X$
- N° 2 - $d1:Z$ $r1:L$
- N° 3 - $d1:Z$ $r1:H$
- N° 4 - $d1:Z$ $r1:X$
- N° 5 - $d1:0$ $d2:1$ $d3:0$ $r1:X$
- N° 6 - $d1:1$ $d2:0$ $d3:1$ $r1:X$
- ...

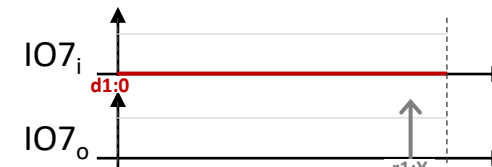
Edges Position

- $d1$: Ons
- $d2$: $CP_ref - \text{setup_time}$ or before
- $d3$: $CP_ref + \text{hold_time}$ or after
- $r1$: $CP_ref + \text{prop_delay}$ or after

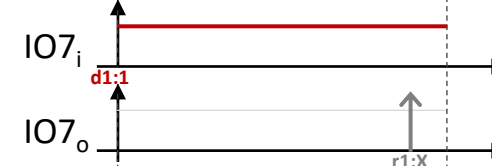
TIMING PROGRAMMING



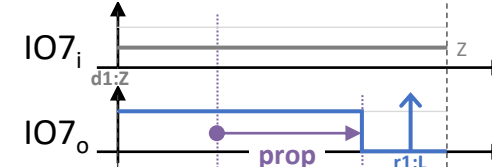
IO7 Waveform N° 0



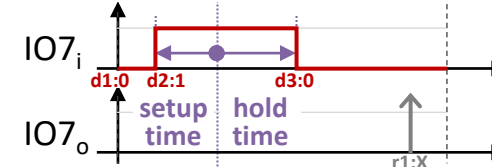
IO7 Waveform N° 1



IO7 Waveform N° 2



IO7 Waveform N° 5



Waveform Name

Programming – I/O Pins

Waveforms

- N° 0 - d1:0 r1:X
- N° 1 - d1:1 r1:X
- N° 2 - d1:Z r1:L
- N° 3 - d1:Z r1:H
- N° 4 - d1:Z r1:X
- N° 5 - d1:0 d2:1 d3:0 r1:X
- N° 6 - d1:1 d2:0 d3:1 r1:X
- ...

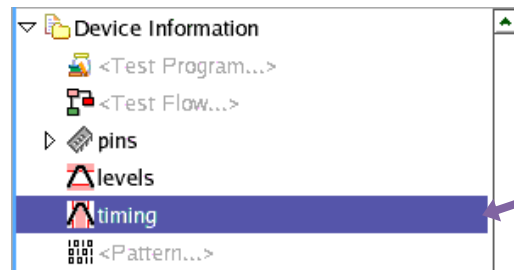
Dev Cycle

- "0"
- "1"
- "L"
- "H"
- "X"
- "SBC_1"
- "SBC_0"

Edges Position

- d1: 0ns
- d2: $\text{CP_ref} - \text{setup_time}$ or before
- d3: $\text{CP_ref} + \text{hold_time}$ or after
- r1: $\text{CP_ref} + \text{prop_delay}$ or after

TIMING SETTING IN SMARTTEST



In the Test Program Explorer

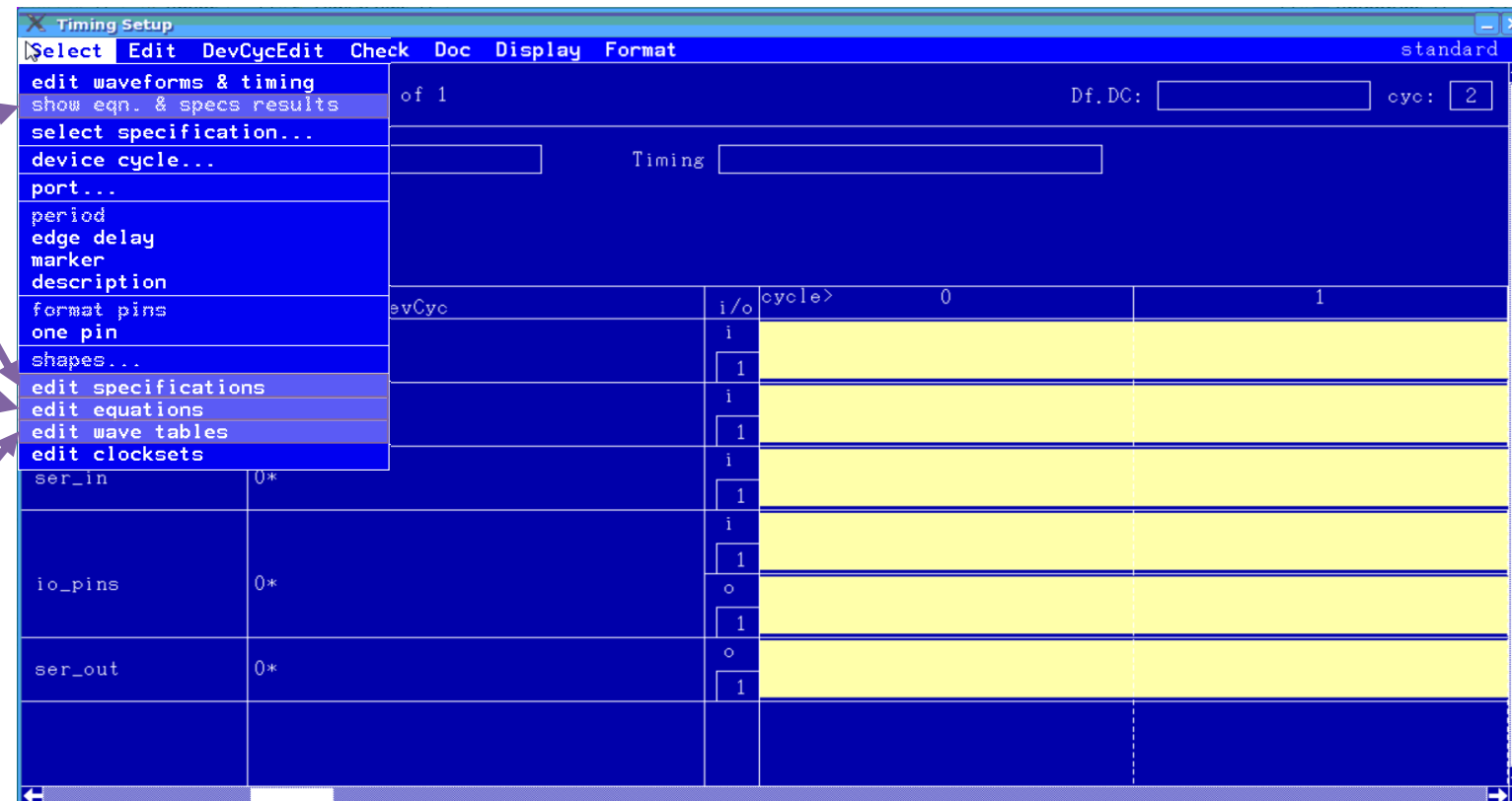
1. Load timing file
2. Open or Double-click on the timing item

Visualize Waveforms

Open SpecTool
Window

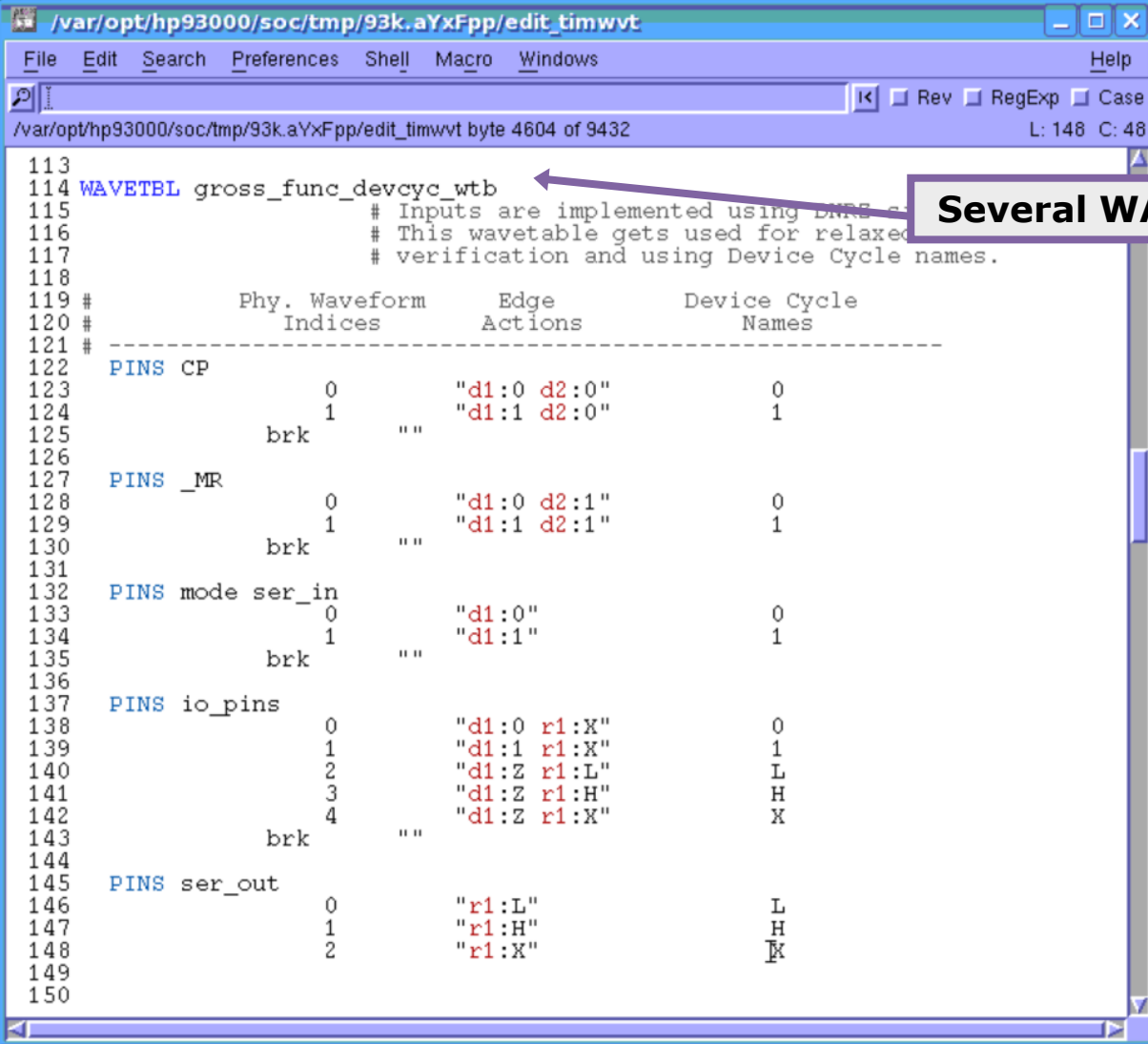
Open EQN SET
Editor

Open WAVETABLE
Editor



TIMING SETTING IN SMARTTEST

WAVETABLE EDITOR



The screenshot shows a text editor window titled "/var/opt/hp93000/soc/tmp/93k.aYxFpp/edit_timwvt". The window contains a table defining waveforms for a device cycle. The table has four columns: "Phy. Waveform Indices", "Edge Actions", and "Device Cycle Names". The table is divided into sections by "PINS" labels: "CP", "_MR", "mode ser_in", "io_pins", and "ser_out". Each section contains a list of indices, edge actions, and device cycle names. A callout box points to the "WAVETBL" line, stating "Several WAVETBLs can exist". A bracket on the right side of the table is labeled "Definition of waveforms".

```
113
114 WAVETBL gross_func_devcyc_wtb
115 # Inputs are implemented using DMS
116 # This wavetable gets used for relaxed
117 # verification and using Device Cycle names.
118
119 #          Phy. Waveform      Edge          Device Cycle
120 #          Indices            Actions          Names
121 # -----
122 PINS CP
123         0          "d1:0 d2:0"          0
124         1          "d1:1 d2:0"          1
125         brk        ""
126
127 PINS _MR
128         0          "d1:0 d2:1"          0
129         1          "d1:1 d2:1"          1
130         brk        ""
131
132 PINS mode ser_in
133         0          "d1:0"              0
134         1          "d1:1"              1
135         brk        ""
136
137 PINS io_pins
138         0          "d1:0 r1:X"          0
139         1          "d1:1 r1:X"          1
140         2          "d1:Z r1:L"          L
141         3          "d1:Z r1:H"          H
142         4          "d1:Z r1:X"          X
143         brk        ""
144
145 PINS ser_out
146         0          "r1:L"              L
147         1          "r1:H"              H
148         2          "r1:X"              X
149
150
```

Several WAVETBLs can exist

Definition
of
waveforms

TIMING SETTING IN SMARTTEST

TIMING
EQUATION SET
EDITOR

```
/var/opt/hp93000/soc/tmp/93k.sVSlr8/edit_timeqn
File Edit Search Preferences Shell Macro Windows Help
Find:  ☐ Rev ☐ RegExp ☐ Case
/var/opt/hp93000/soc/tmp/93k.sVSlr8/edit_timeqn 2053 bytes

63
64 EQNSET 2 "spec_search_eqn"
65
66 SPECS
67 #-----
68 #   Spec          Unit
69 # variables
70 #-----
71
72 f [MHz]
73 ts_Sx_CP [ns]
74 th_CP_Sx [ns]
75 ts_IOx_CP [ns]
76 th_CP_IOx [ns]
77 ts_DSx_CP [ns]
78 th_CP_DSx [ns]
79 tw_CP [ns]
80 tw_MR [ns]
81 trec_MR_CP [ns]
82 tpd_CP_Qx [ns]
83 tpd_CP_IOx [ns]
84
85 EQUATIONS
86
87 p = 1/f*1000
88 CP_ref = p/2
89 ComplDelay = 2
90
91 TIMINGSET 1 "std"
92
93 period = p
94
95 PINS CP
96 d1 = CP_ref
97 d2 = CP_ref + tw_CP
98
```

Several EQNSETs can exist

Values are assigned to Spec variables
in the Spec ToolAdditional variables can be defined
with equations that use Spec variables

Several TIMINGSETs can exist

Values can be expressed
with variables

TIMING SETTING IN SMARTEST

```
/var/opt/hp93000/soc/tmp/93k.sVSIr8/edit_timeqn
File Edit Search Preferences Shell Macro Windows Help
Find: [ ] Rev [ ] RegExp [ ] Case
/var/opt/hp93000/soc/tmp/93k.sVSIr8/edit_timeqn 2053 bytes

63
64 EQNSET 2 "spec_search_eqn"
65
66 SPECS
67 #-----
68 # Spec Unit
69 # variables
70 #-----
71 f [MHz]
72 ts_Sx_CP [ns]
73 th_CP_Sx [ns]
74 ts_IOx_CP [ns]
75 th_CP_IOx [ns]
76 ts_DSx_CP [ns]
77 th_CP_DSx [ns]
78 tw_CP [ns]
79 tw_MR [ns]
80 trec_MR_CP [ns]
81 tpd_CP_Qx [ns]
82 tpd_CP_IOx [ns]
83
84 EQUATIONS
85
86 p = 1/f*1000
87 CP_ref = p/2
88 ComplDelay = 2
89
90 TIMINGSET 1 "std"
91
92 period = p
93
94 PINS CP
95 d1 = CP_ref
96 d2 = CP_ref + t
97
98
```

SpecTool

File Select Change Edit Sort Display Doc Help

Timing

Specification [2] [2] spec_search_logical_specs

Wavetable [spec_search_logical_wtb] **Select a Wavetable**

Equation [2] spec_search_eqn **Enter Values**

Name	Actual	Minimum	Maximum	Measured	Unit	Comment
f	50				MHz	
ts_Sx_CP	7	3	10		ns	
th_CP_Sx	1	-4	2		ns	
ts_IOx_CP	4	1.5	5		ns	
th_CP_IOx	1.2	-1	2		ns	
ts_DSx_CP	4.5	1.5	6		ns	
th_CP_DSx	1.5	-2	2		ns	
tw_CP	4	0	5		ns	
tw_MR	3.5	1	5		ns	
trec_MR_CP	3	0.5	5		ns	

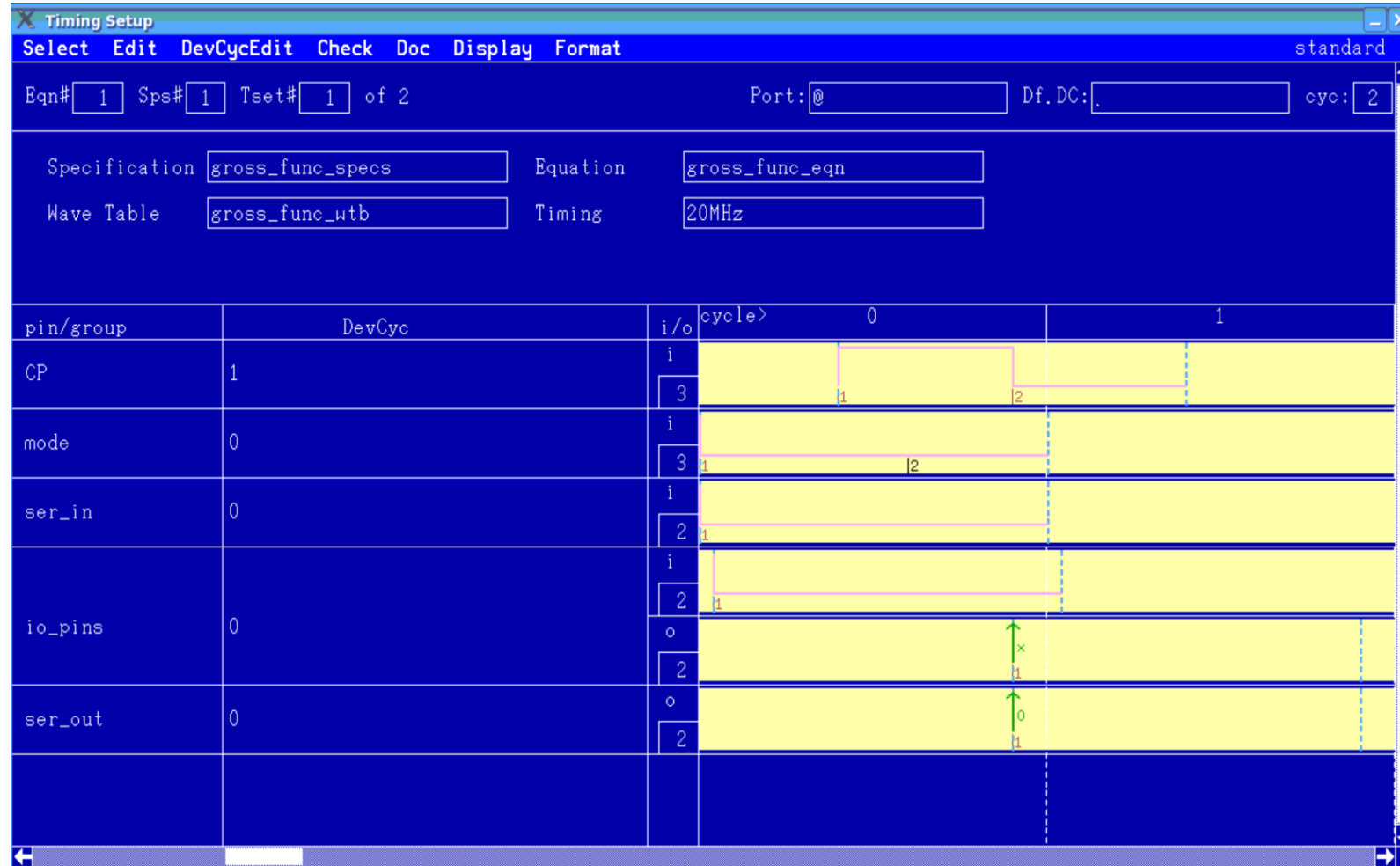
Download done!

TIMING
SPEC TOOL

TIMING SETTING IN SMARTTEST

Waveform Visualization

"Show eqn. & Specs Results"



View with **"format pins"** active, i.e. only one waveform displayed for each pin or pin group

To see all waveforms defined for a given pin or pin group, click on the name of a pin or pin group and choose **"one pin"**

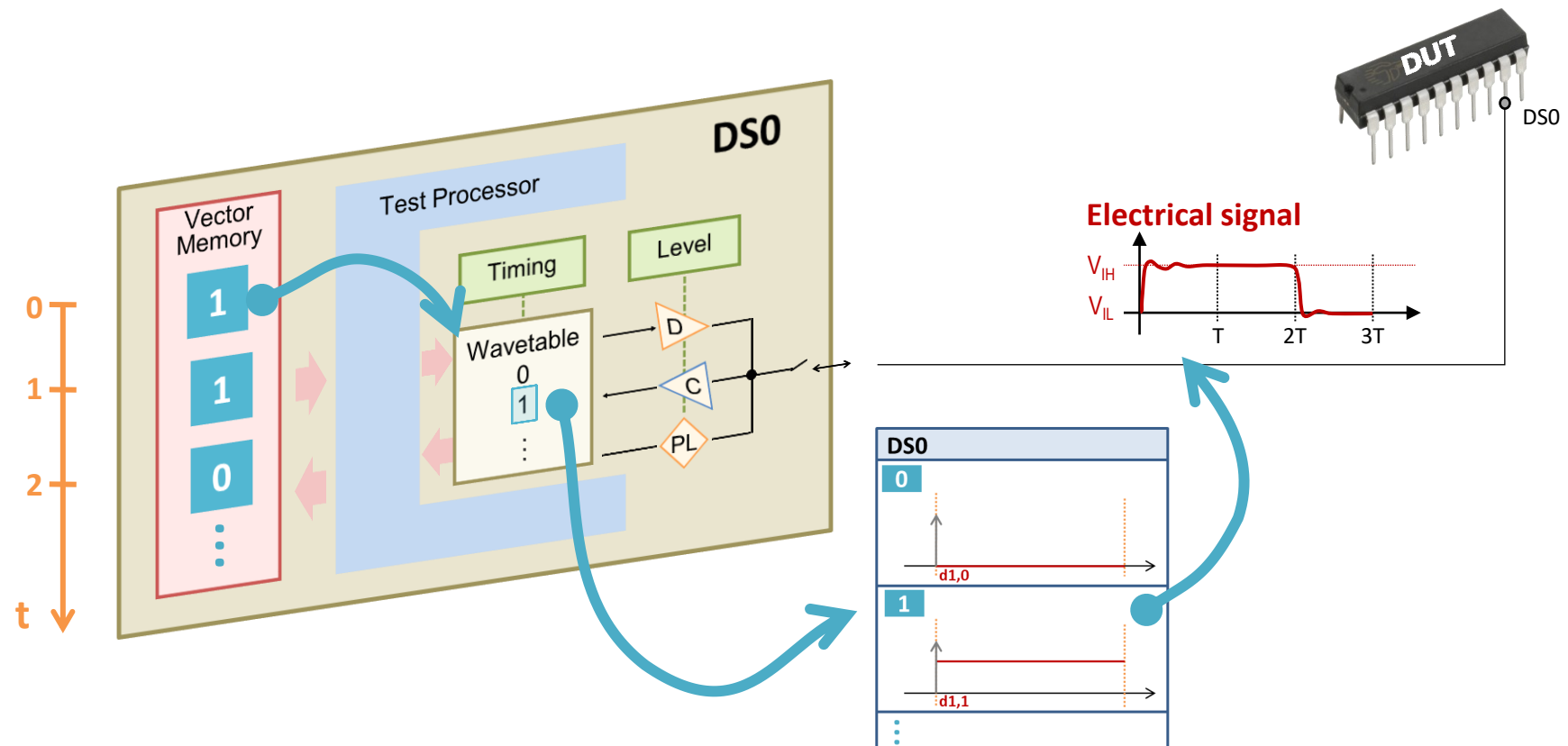
Select Edit DevCycEdit Che
edit waveforms & timing
show eqn. & specs results
select specification...
device cycle...
port...
period
edge delay
marker
description
format pins
one pin
shapes...
edit specifications
edit equations
edit wave tables
edit clocksets



PATTERN

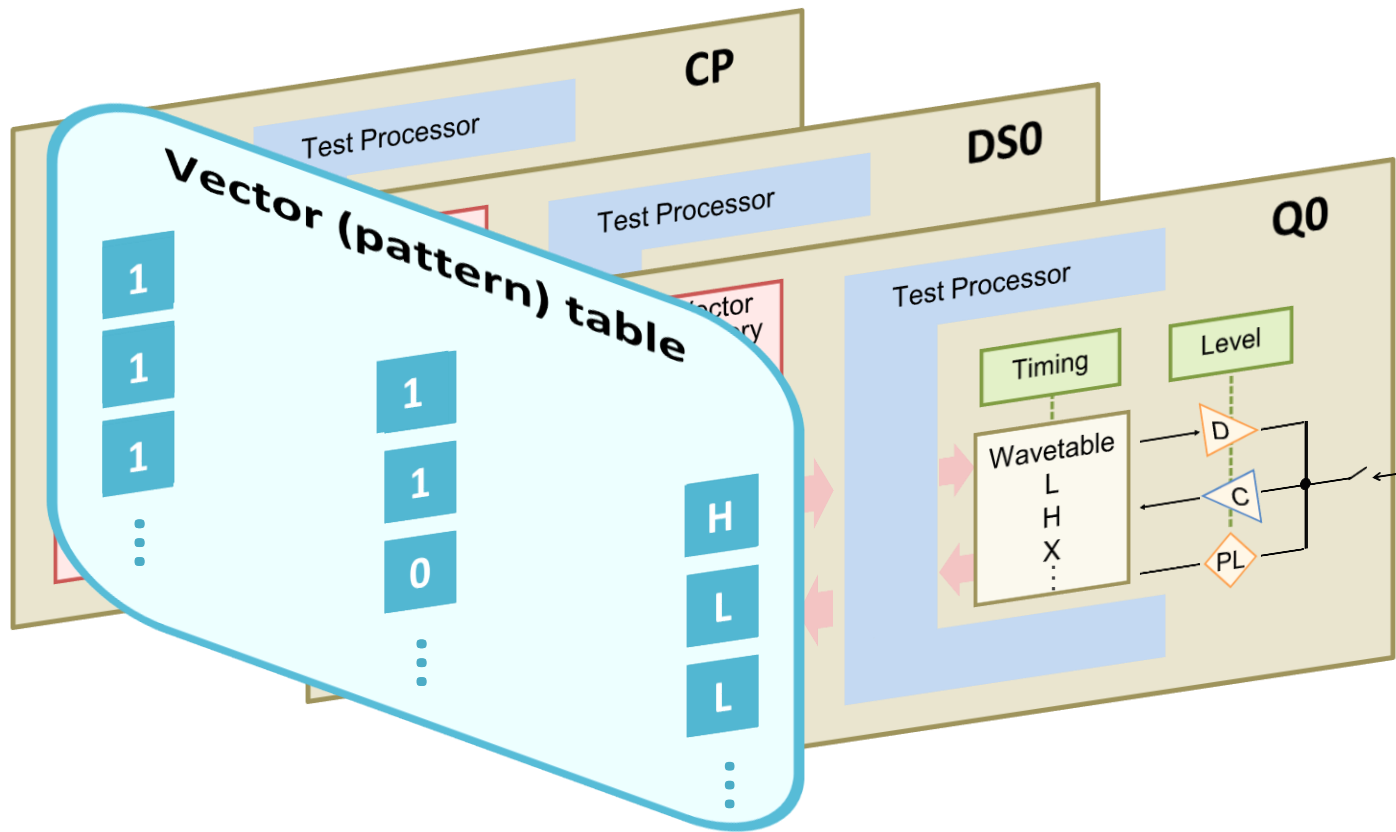
- Principle

- Sequence of waveform indexes/names that will be “played” by the test processor



PATTERN

- Principle
 - Sequence of waveform indexes/names that will be “played” by the test processor



- Data in the pattern table do not directly correspond to a logic value but refer to a waveform index or name
- Pattern cannot be defined before timing (waveforms must exist before referring to them)

PATTERN TOOL IN SMARTEST

The screenshot displays the SmartTest Eclipse Workcenter interface. The top menu bar includes File, Edit, Navigate, Search, Project, Run, 93000, Window, and Help. The left sidebar shows a tree view of the project structure, with 'pins_soc' expanded and 'all binl' selected. The main window is divided into two panes. The top pane, titled 'Pattern Editor: display one pattern', shows a table of test vectors. The bottom pane, titled 'Pattern Explorer: list all patterns', shows a list of patterns.

Pattern Editor: display one pattern

Signal	CP (DVC)	DS0 (DVC)	DS7 (DVC)	I/O0 (DVC)	I/O2 (DVC)	I/O3 (DVC)	I/O4 (DVC)	I/O5 (DVC)	I/O6 (DVC)	I/O7 (DVC)	S0 (DVC)	S1 (DVC)	MR (DVC)
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	X	X	X	X	X	X	X	0	0	1
2	1	0	0	1	0	0	0	0	0	0	H	L	1
3	1	0	0	L	H	L	L	L	L	L	L	1	0
4	1	0	0	L	H	L	L	L	L	L	L	1	0
5	1	0	0	L	L	H	H	L	L	L	L	0	1
6	1	0	0	L	H	H	L	L	L	L	L	0	1
7	1	0	0	L	H	H	L	L	L	L	L	0	1
8	1	0	0	H	H	L	L	L	L	L	H	0	1
9	1	0	0	L	L	L	L	L	L	L	L	0	1
10	1	0	0	X	X	X	X	X	X	X	L	0	0
11	1	0	0	1	0	1	0	1	0	1	H	1	1
12	1	0	0	H	H	L	H	L	H	L	H	0	0
13	1	0	0	L	H	L	H	L	H	L	L	0	1
14	0	0	X	X	X	X	X	X	X	X	X	0	0
15	1	0	0	X	X	X	X	X	X	X	X	0	0
STOP													

Pattern Explorer: list all patterns

Name	Port	Type	Memory	WaveTable	Layout
Burst	@	Burst	NONE	gross_func_wtb	
func_tirst	@	Main	VM	gross_func_dev...	
gross_burst	@	Burst	NONE	gross_func_wtb	
gross_func	@	Main	VM	gross_func_wtb	abc
gross_func_fail	@	Main	VM	gross_func_dev...	abc
p1	@	Main	VM	gross_func_wtb	
p2	@	Main	VM	gross_func_dev...	
p3	@	Main	VM	gross_func_wtb	
p4	@	Main	VM	gross_func_wtb	
spec_search	@	Main	VM	spec_search_wtb	

1. In the Test Program Explorer, double-click on the pattern item

2. In the Pattern Explorer, double-click on one pattern

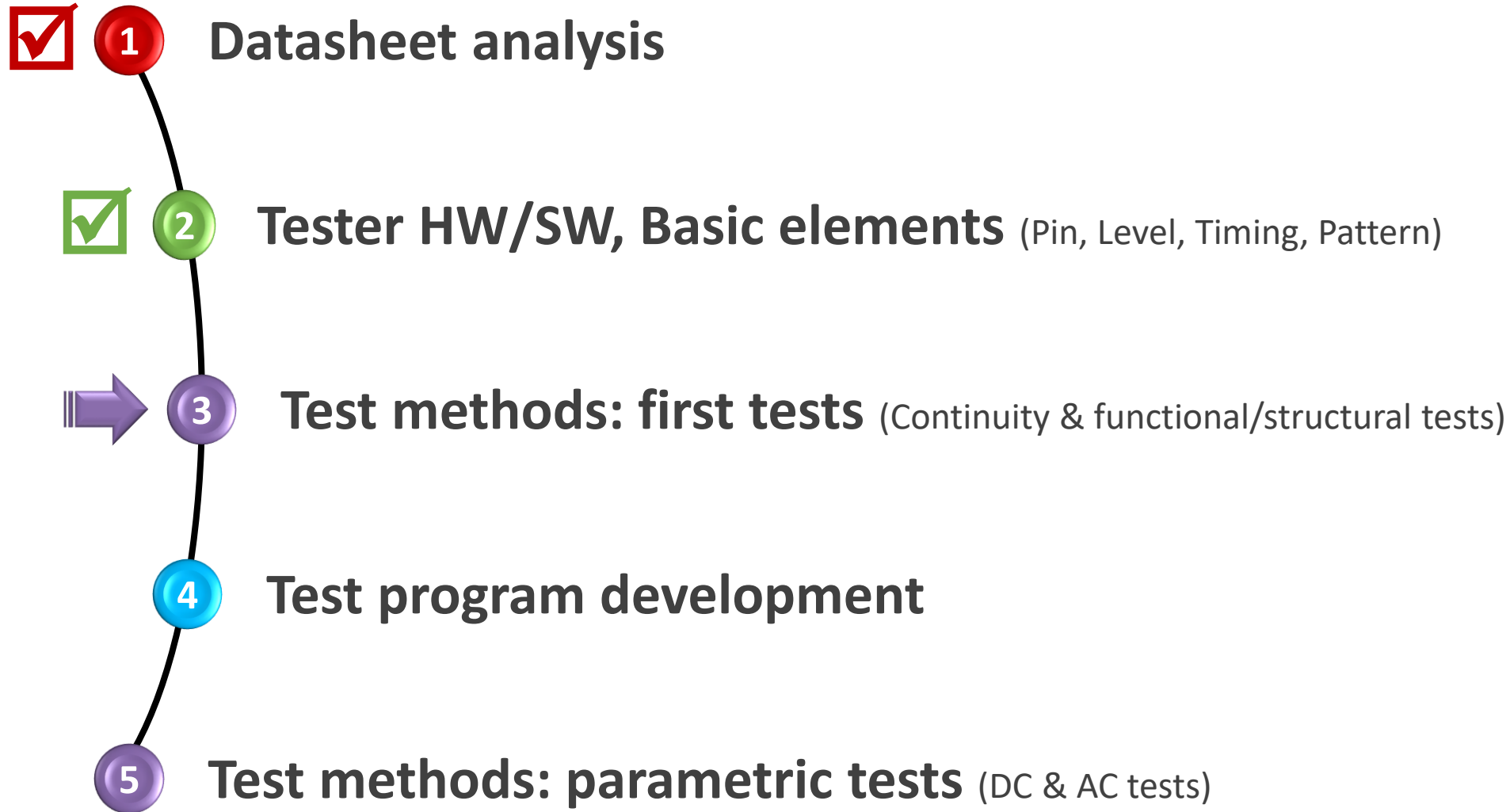
Pattern Explorer: list all patterns



Lab & Exercises: First Steps with SmarTest - Part 2



LEARNING STEPS



PART 3

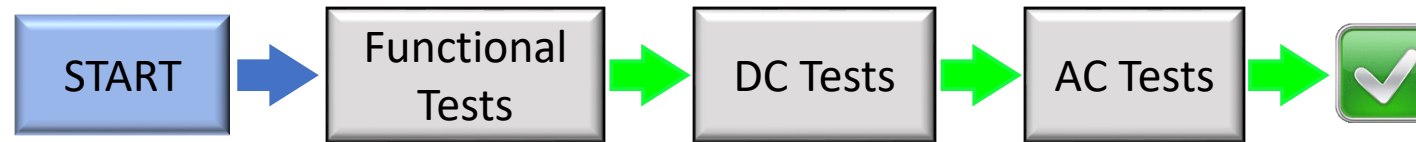


TEST METHODS

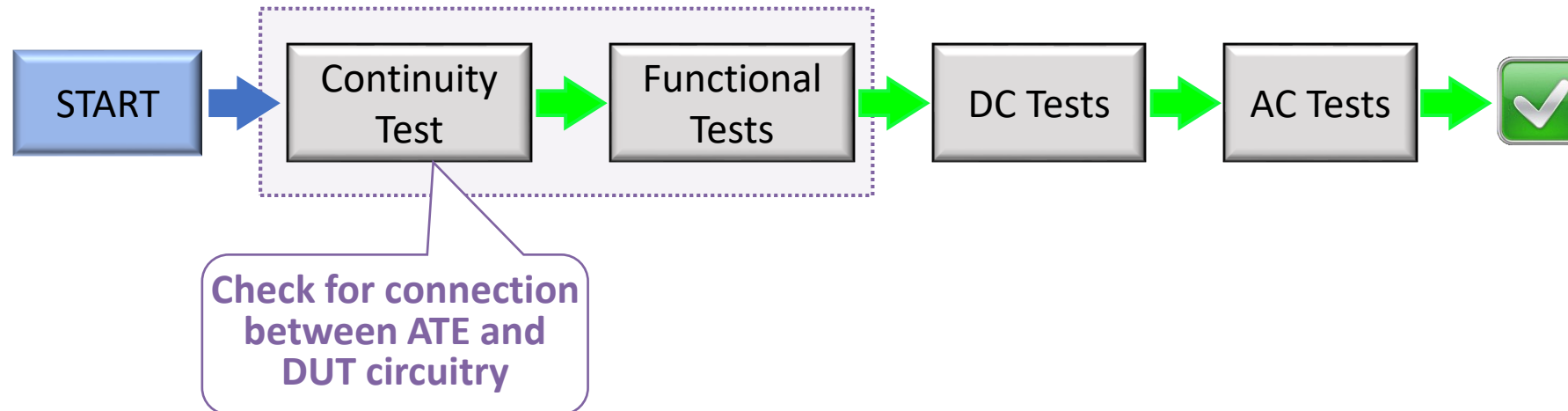
- Continuity Test
- Functional/Structural Tests

TEST METHODS: FIRST TESTS

- Test Flow planned from Datasheet Analysis



- Actual Production Test Flow

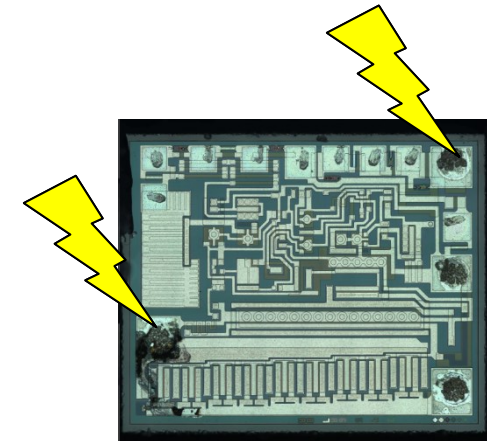
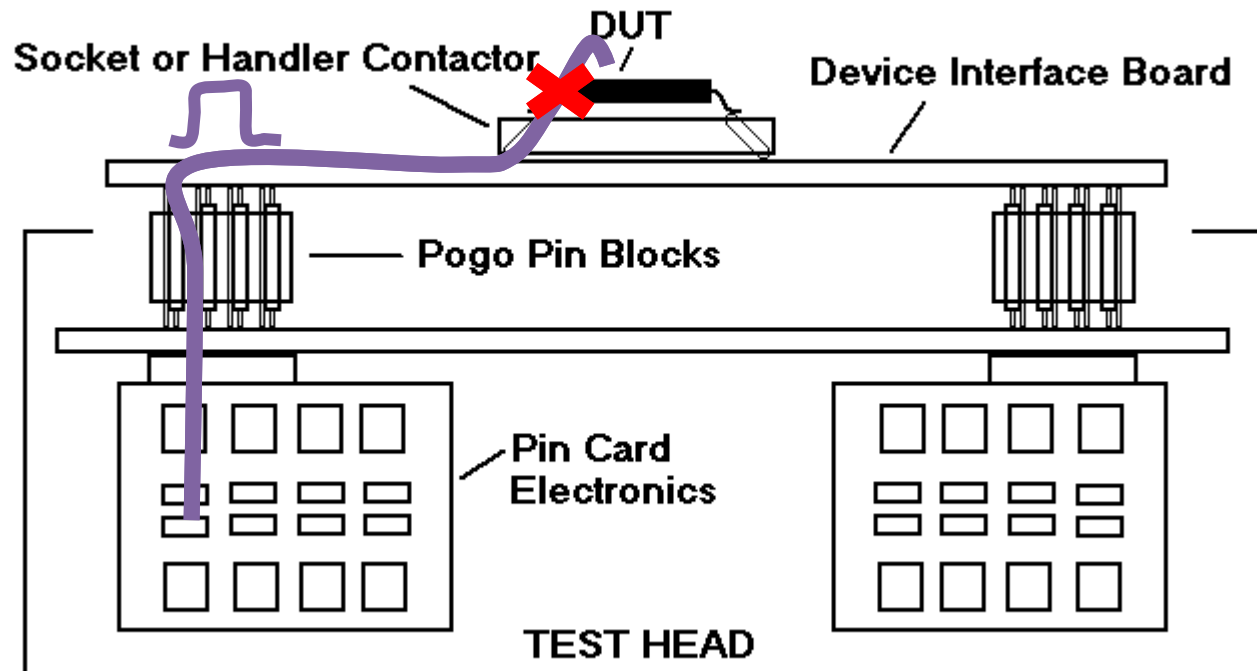


CONTINUITY TEST

(also called “Open/Short Test” or “Contact Test”)

- Purpose

- Verify the connection between ATE and DUT pins (no open)
- Verify that no DUT pin is shorted to power/ground



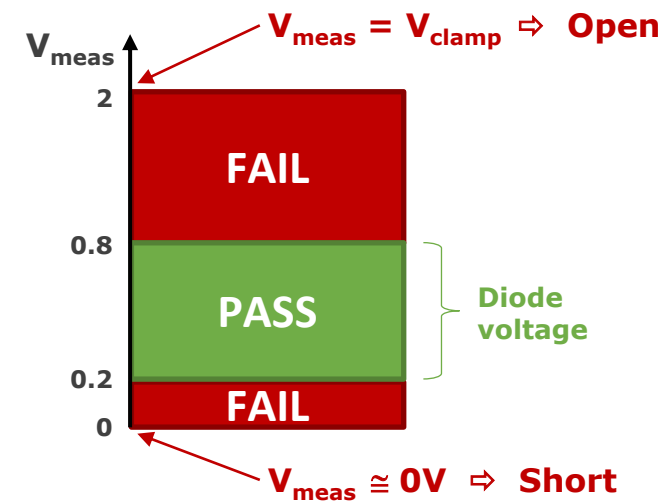
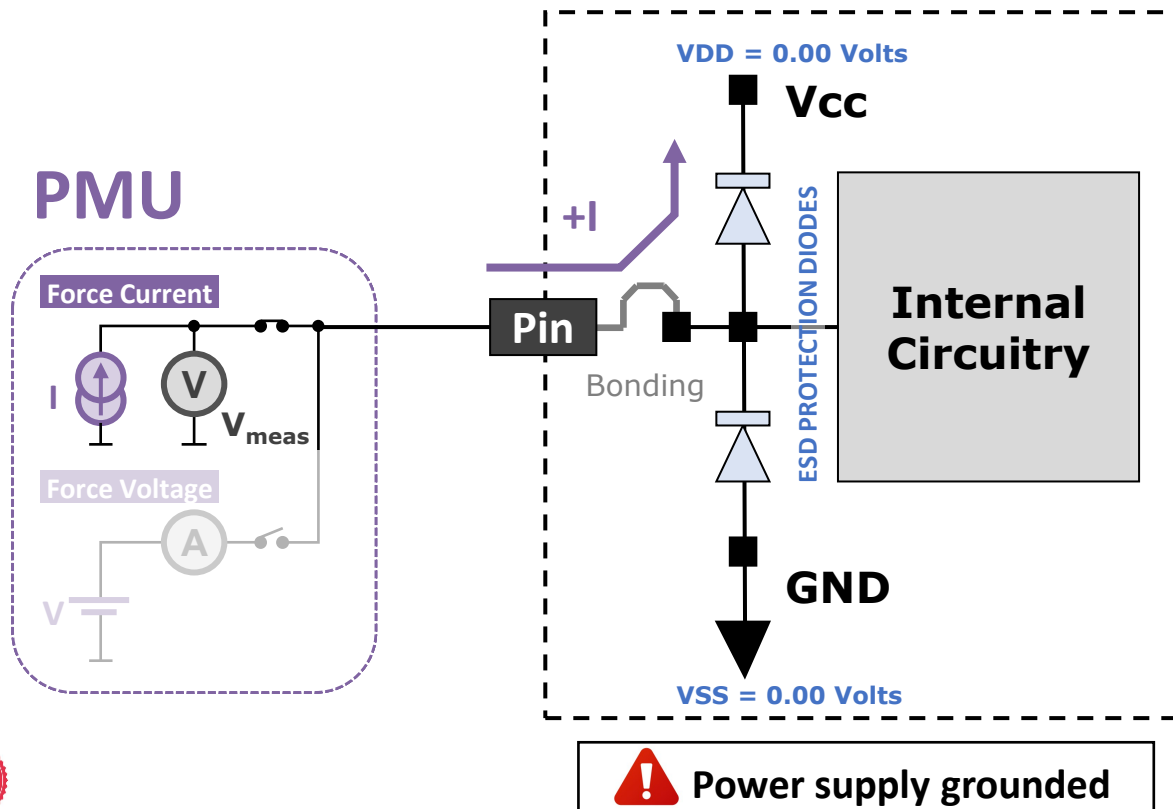
No ESD damage

CONTINUITY TEST

(also called “Open/Short Test” or “Contact Test”)

- Principle

- **Force I & Measure V:** resulting voltage should be a diode voltage (ESD protection diodes)

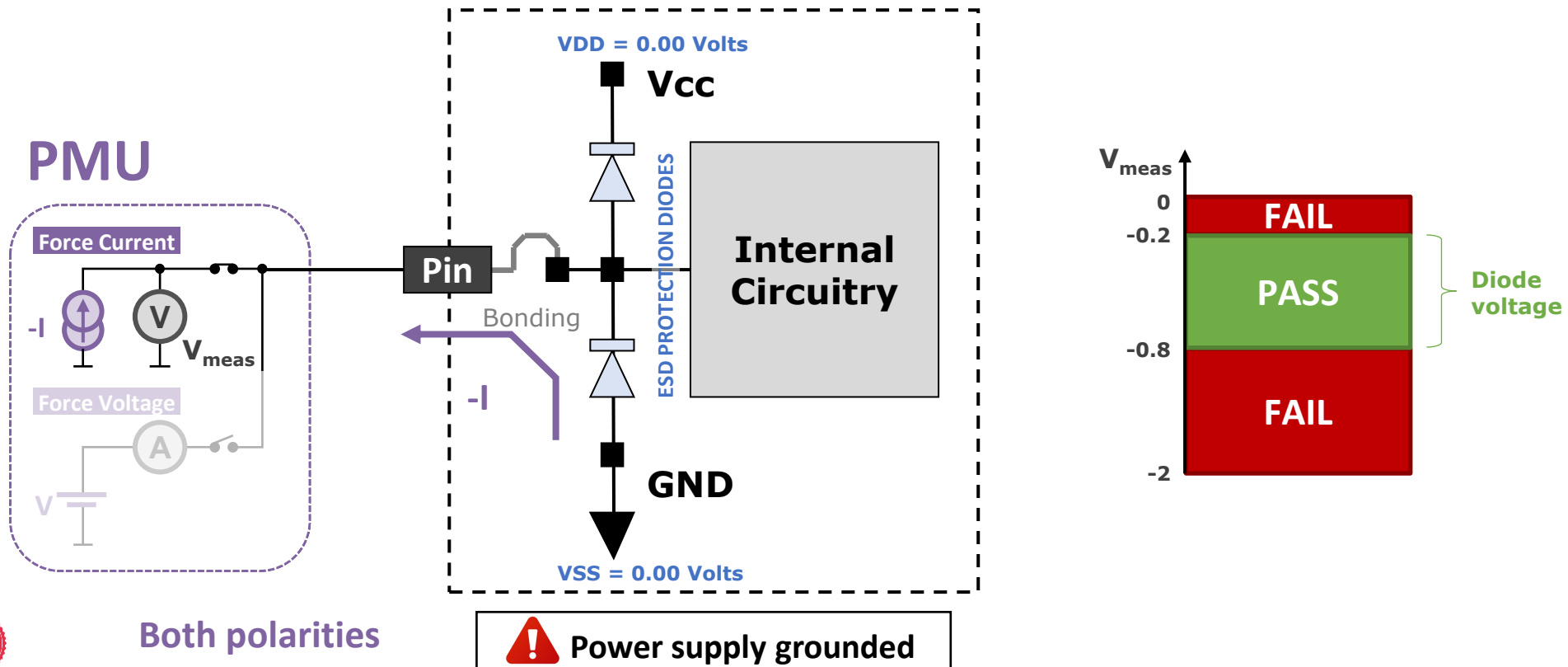


CONTINUITY TEST

(also called “Open/Short Test” or “Contact Test”)

- Principle

- **Force I & Measure V:** resulting voltage should be a diode voltage (ESD protection diodes)

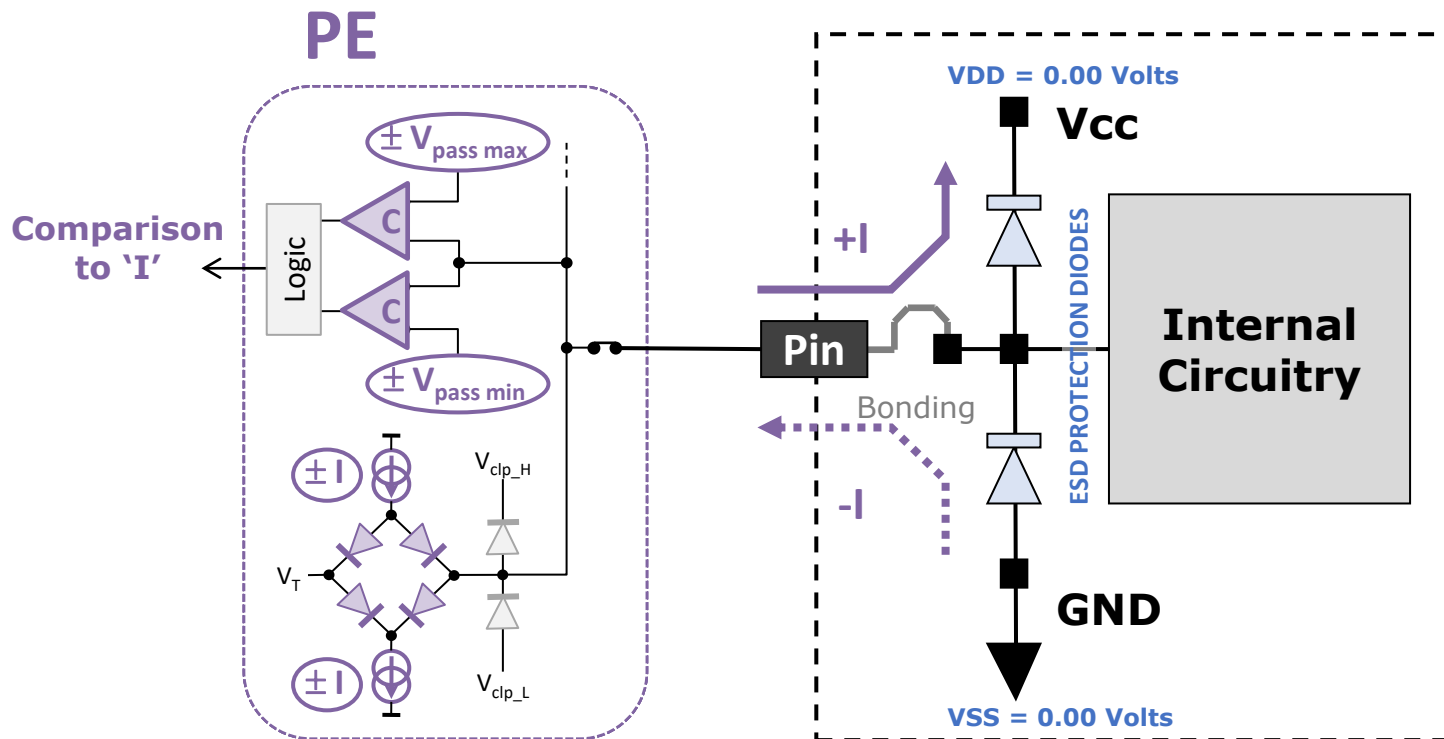


CONTINUITY TEST

(also called “Open/Short Test” or “Contact Test”)

- Principle

- **Force I & Measure V:** resulting voltage should be a diode voltage (ESD protection diodes)



**Other option:
Implementation with
Programmable Load (PL)**



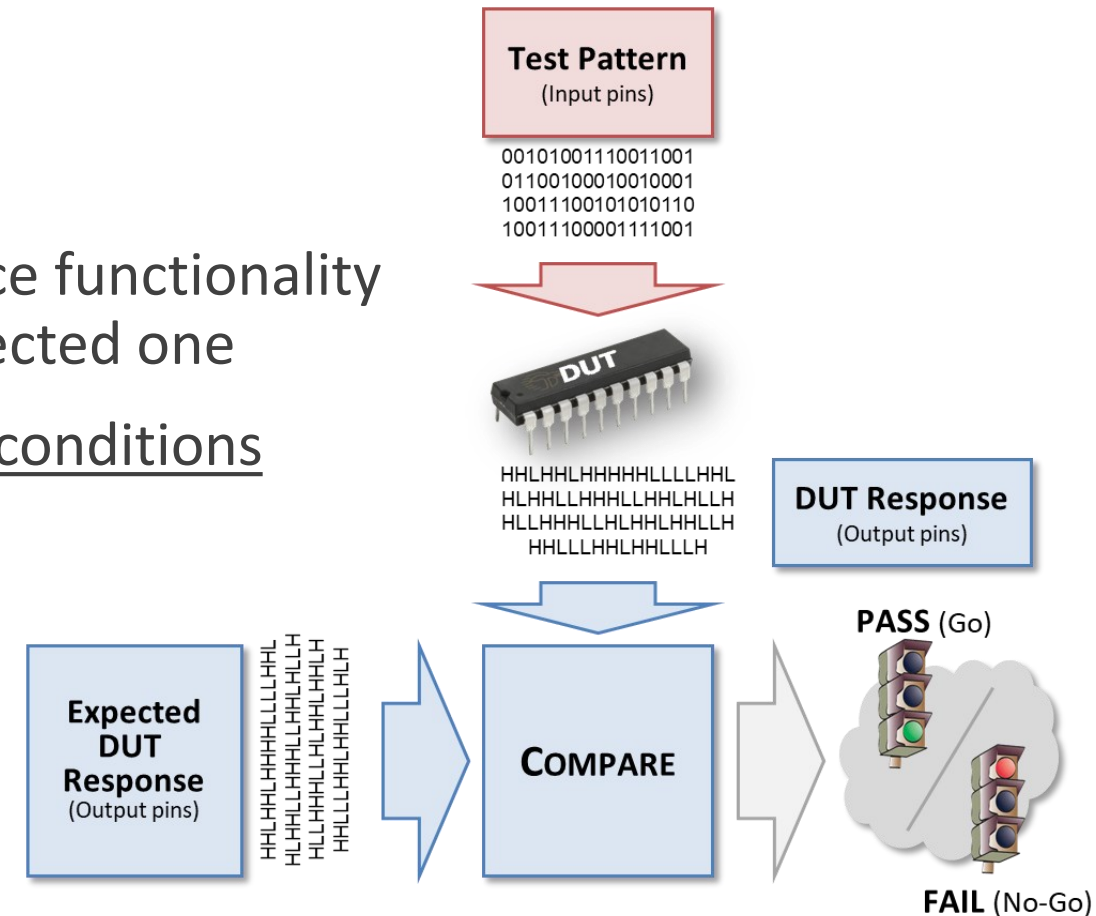
no Meas. Value
Pass/fail result only

FUNCTIONAL TEST

- Purpose
 - Verify that the DUT is functionally “alive”
- Principle
 - Apply a test pattern that exercises the device functionality & compare the DUT response with the expected one
 - Test performed with relaxed level & timing conditions

- $V_{IL} = 0V, V_{IH} = V_{CC}$
- $V_{OL} = \frac{V_{CC}}{2} - 10\% * V_{CC}, V_{OH} = \frac{V_{CC}}{2} + 10\% * V_{CC}$
- $f < f_{max}$
- $T_{setup} > T_{setup-DS}, T_{hold} > T_{hold-DS}$
- $T_{obs} > T_{prop-DS}$

- Output: PASS/FAIL result



FUNCTIONAL VS. STRUCTURAL TEST APPROACH

FUNCTIONAL

- Test pattern is defined with the objective to **exercise the device functionality**
 - “manual” generation based on the knowledge of the truth table

Inputs				Response
MR	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ –Q ₇ = LOW
H	H	H	✓	Parallel Load; I/O _n → Q _n
H	L	H	✓	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	✓	Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold



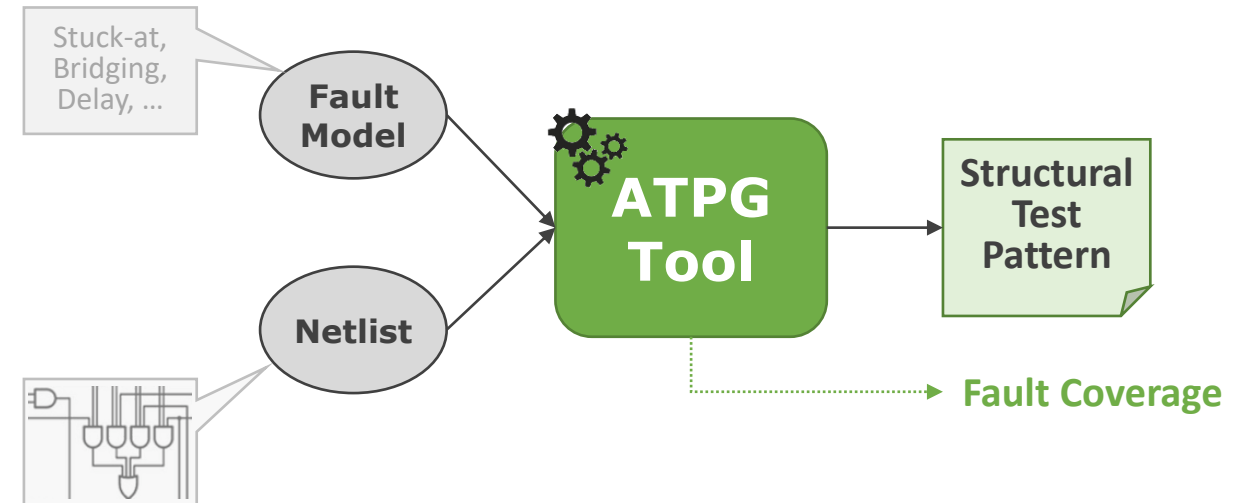
Master reset
Hold
Parallel Load (10000000)
Hold
Shift Right x8 – DS0=0
Parallel Load (01010101)
Shift Left x8 – DS7=1
...



**Functional
Test
Pattern**

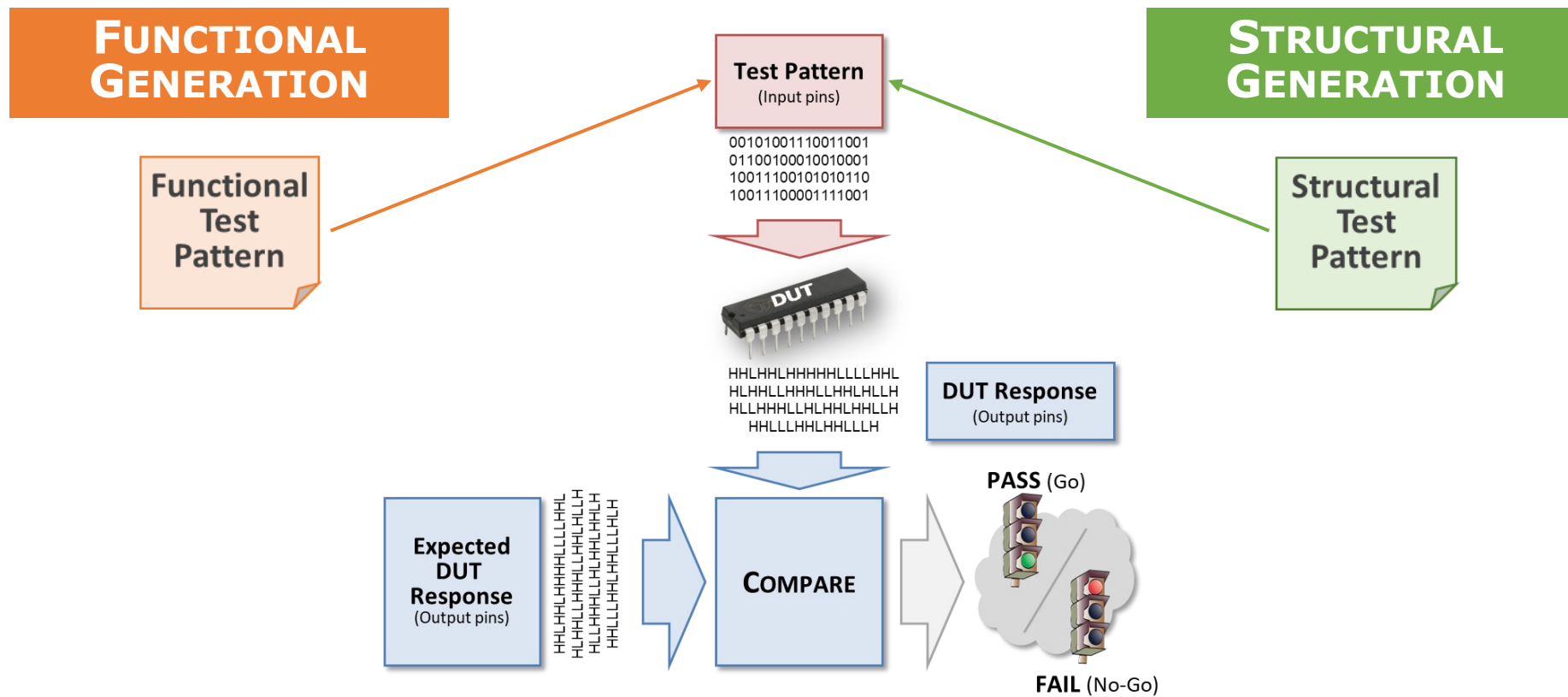
STRUCTURAL

- Test pattern is defined with the objective to **verify the absence of defects**
 - automatic generation based on fault models & structural circuit description



FUNCTIONAL VS. STRUCTURAL TEST APPROACH

- Execution on ATE: no fundamental difference



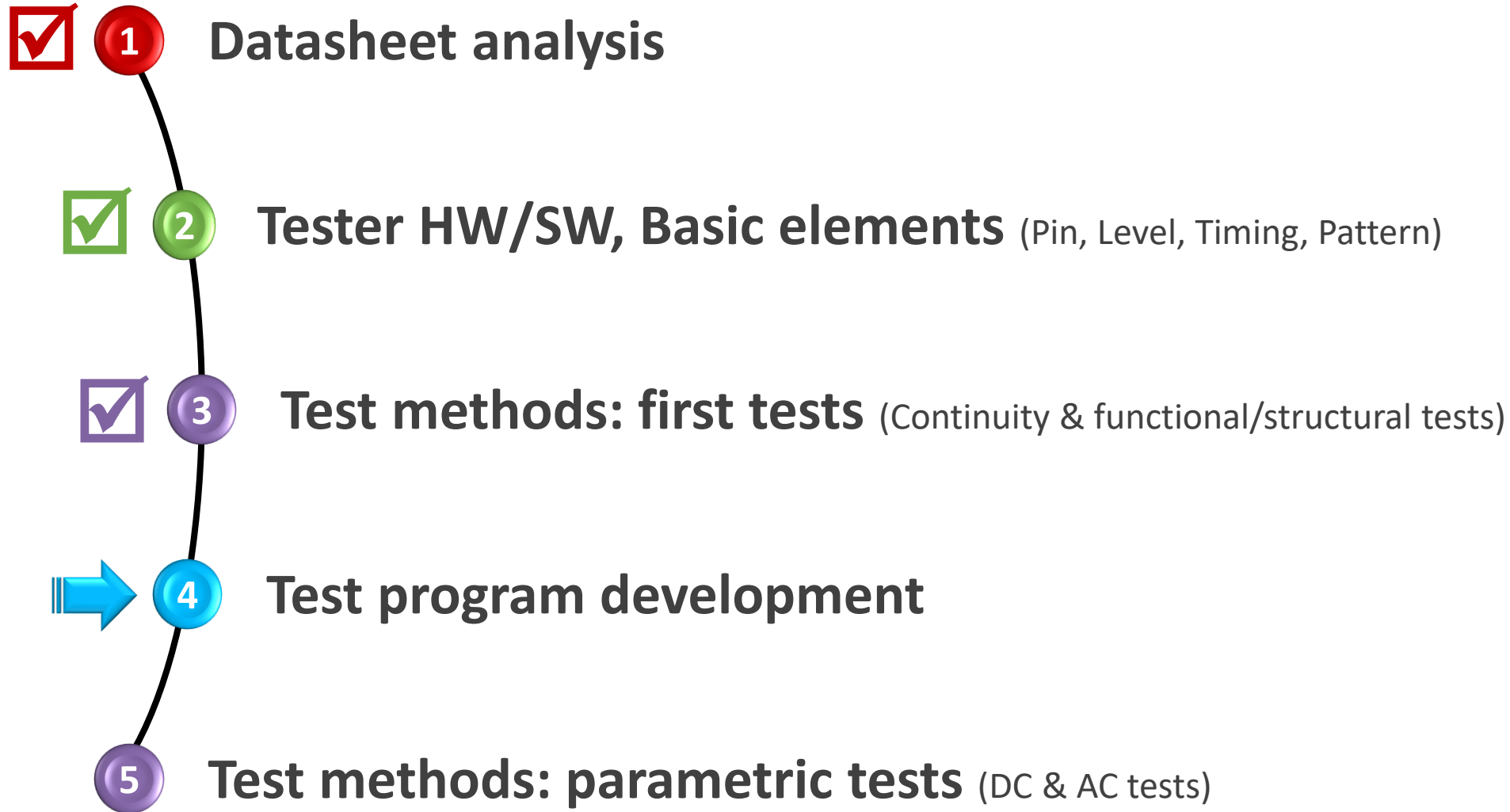


Exercise:



Questions about First Test Concepts

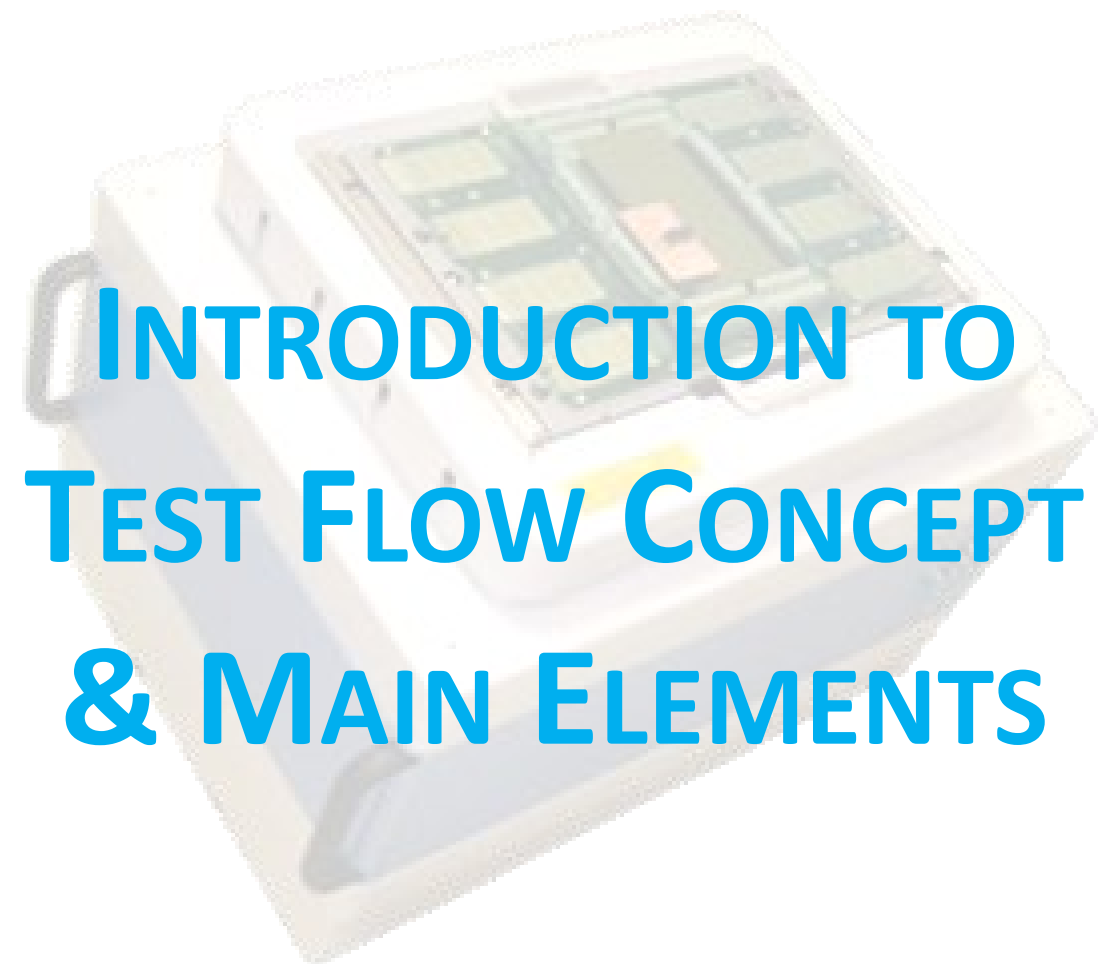
LEARNING STEPS



PART 4



- **Test Flow Concept & Main Elements**
- **Test Flow Creation & Execution in SmarTest**



- Sequential organization of device tests with their bins
- Tests order, pass/fail branching and binning determine the execution of the test flow

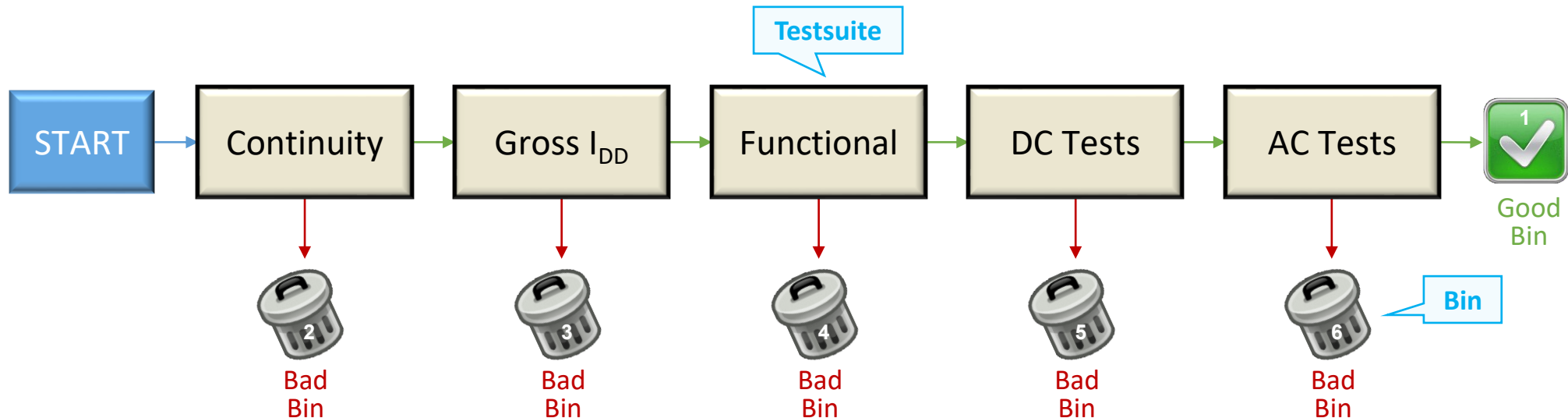
Main Test Flow Elements

Testsuites

- Test Method + Level/Timing/Pattern Settings

Bins

- Good or Bad (*STOP* point)



- Sequential organization of device tests with their bins
- Tests order, pass/fail branching and binning determine the execution of the test flow

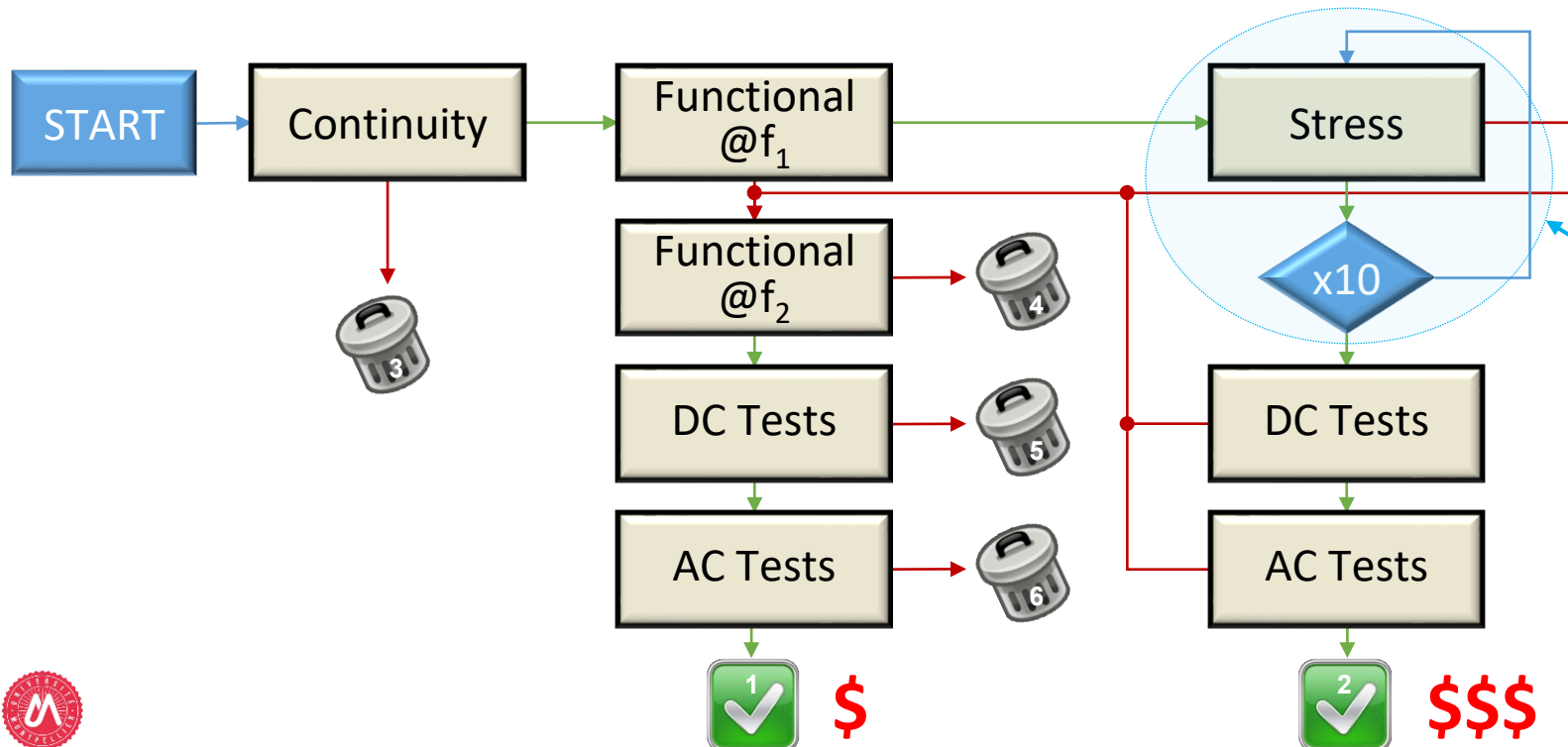
Main Test Flow Elements

Testsuites

- Test Method + Level/Timing/Pattern Settings

Bins

- Good or Bad (*STOP* point)



Other Test Flow Elements

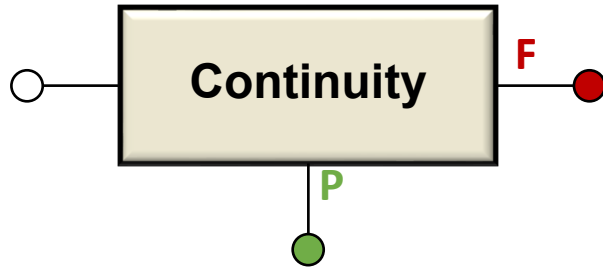
Iterative/Conditional Elements

- Repeat Loop
- For Loop
- While Loop
- If/Then

Value Assignments

- Variable
- Level value
- Timing value

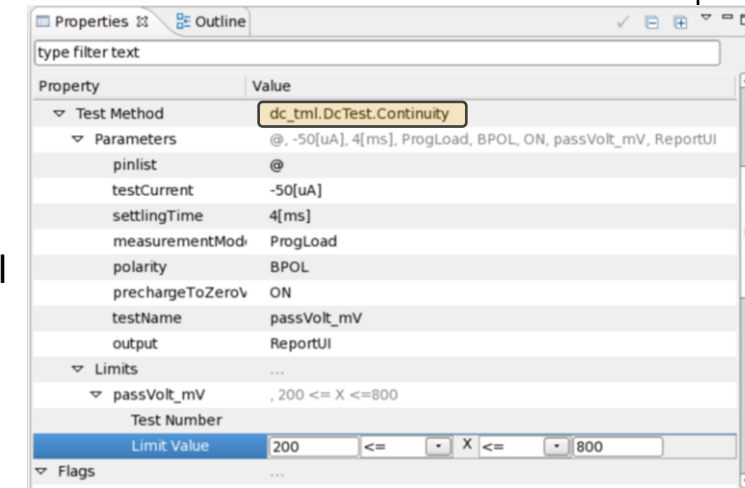
TESTSUITE



Property	Value
▼ Testsuite	Continuity
▷ Test Method	"DcTest.Continuity"
▼ Primaries	
▷ Timing	1.2.1
▷ Level	2.2.1
▷ Pattern	my_pattern

TEST METHOD

- 2 ways of calling a test method
 - Predefined "Test Function"
 - Only test conditions and limits to fill
 - Hidden firmware code, the user can't modified
 - Easy to understand for beginners
 - C/C++ code
 - The user programs test conditions, tester HW (relays), test execution, comparison to test limits, test result reporting and P/F outcome
 - Not easy to implement, more flexibility



```

HRESULT digital_tests::continuity(double _results[4])
{
    // add your code
    PPMU_SETTING setting1;
    setting1.pin("G").iForce(50 uA).min(50 mV).max(100 mV).iRange("100uA");
    PPMU_RELAY relay1, relay2;
    relay1.pin("G").status("PPMU_ON");
    relay1.wait(1.3 ms);
    //DISCONNECT PPMU relays
    relay2.pin("G").status("ALL_OFF");
    relay2.wait(1.3 ms);
    PPMU_MEASURE meas1;
    meas1.pin("G").execMode(TM::PVAL);
    TASK_LIST task1;
    task1.add(setting1).add(relay1).add(meas1).add(relay2);
    task1.execute();
    return S_OK;
}

```

Set up: pin to test, force current and limits

Close PPMU relay

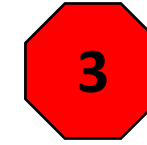
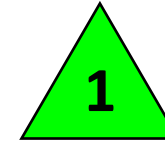
Open PPMU relay

Test technique: value

Task list execution order:

1. Apply setup
2. Close PPMU relay
3. Perform measurements on pins
4. Open PPMU relay

GOOD/BAD BIN



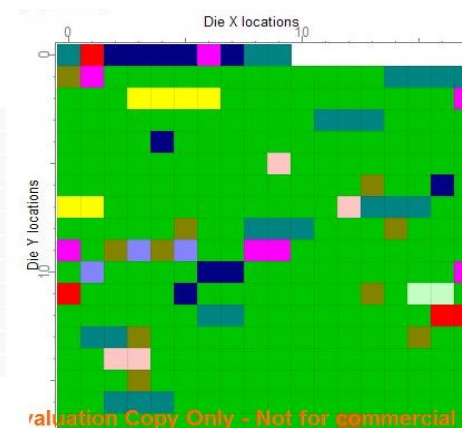
- To sort the devices
- Hardware and software bin numbers defined in the test program
 - Hardware bin number: controls the location where the DUT will be placed (tray or tube) after execution of the test program
 - Software bin number: keeps track of the various pass/fail categories (Statistics)

List of Individual Maps

...Evaluation Copy Only - Not for commercial use...

Top 10 Software Binning	1	1004	1400	1630	601	600	1110	500	700	Others
	PASS	thunderbird_real_bist_max	vil_vih_voh_max	idd_sleep_max	thunderbird_ct_max	thunderbird_ic_max	cont_pwr	thunderbird_ic_min	lvdsTest070731_nom	
Color	Green	Teal	Olive	Dark Blue	Magenta	Yellow	Pink	Red	Blue	-
Pass/Fail	P	F	F	F	F	F	F	F	F	-
Percentage	77.8%	7.3%	3.5%	3.2%	2.2%	1.9%	1.3%	1.3%	0.9%	0.6%
Total count	246	23	11	10	7	6	4	4	3	2

File	D:/Qualtera/Galaxy/P61222.0U_9D00646101_20071228103119.stdf
Map style	STRIP map (parts tested are PACKAGED DEVICES!)
Total physical parts tested	316
Parts processed	All Data / parts (any Bin)
Data from Sites	All sites
Product	om6361
Lot	P61222.0U
SubLot	9D00646101
Strip ID:	P61222.0U-9D00646101
Strip started	ven. déc. 28 13:54:09 2007
Map dimensions	LowX=0, LowY=0, HighX=17, HighY=17



...Evaluation Copy Only - Not for commercial use...

TEST FLOW CREATION & EXECUTION IN SMARTTEST



TEST FLOW CREATION IN SMARTTEST

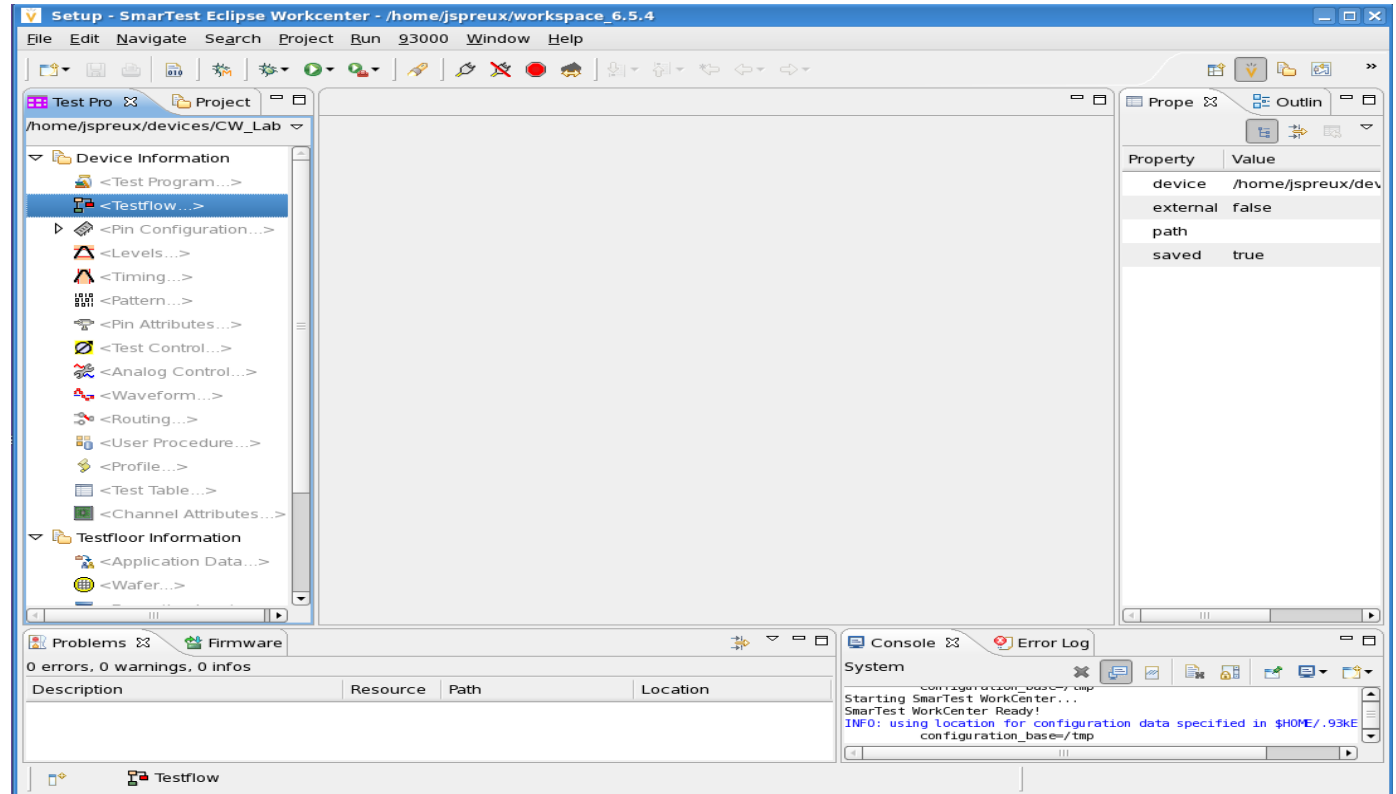
MAIN STEPS

1. Create new testflow

2. Setup the "context"

3. Insert elements
(Testsuites & Bins)

4. Save testflow



1. Create new testflow

TEST FLOW CREATION IN SMARTTEST

1 Right-click on testflow item & Select 'New'

2 Enter name of new testflow

3 Click 'Finish'

4 Right-click on testflow item & Select 'OpenWith -> Flow Sequence Editor'

Empty flow

The image illustrates the process of creating a new test flow in SmartTest. It consists of four numbered steps: 1. Right-clicking on a test flow item in the Project Explorer and selecting 'New'. 2. Entering the name of the new test flow in the 'New Testflow' dialog box. 3. Clicking the 'Finish' button in the 'New Testflow' dialog box. 4. Right-clicking on the test flow item in the Project Explorer and selecting 'OpenWith -> Flow Sequence Editor'. The final result is an 'Empty flow' editor showing a 'Start' block and a 'Palette' on the left.

2. Setup files assignment

TEST FLOW CREATION IN SMARTTEST

1 Right-click in empty zone of 'Flow Sequence Editor'

2 Select 'Open -> Setups Page'

3 Fill in your primary setup files

The image shows two screenshots of the SmartTest software interface. The first screenshot shows the 'Flow Sequence Editor' with a 'Start' button and a 'Palette' on the left. A right-click context menu is open, showing options like 'Run Selected', 'Run Testflow', 'Open', 'Go To', 'Insert', 'Insert Floating Test Suite...', 'Cut', 'Copy', 'Paste', 'Delete', 'Group', 'Ungroup', 'Move', 'Collapse All', 'Expand All', and 'Preferences...'. The 'Open' option is selected, and a sub-menu is shown with 'Variables Page', 'Flags Page', and 'Setups Page'. The 'Setups Page' is highlighted. The second screenshot shows the 'Setups Page' with a table of setup files. The table has columns 'Setup' and 'File'. The 'Setup' column lists items 1 through 10: Pin Configuration, Levels, Timing, Pattern, Pin Attributes, Channel Attributes, Analog Control, Waveform, Routing, and Test Table. The 'File' column shows the corresponding file names: pins, levels, timing, all.binl, all.binl, and all.binl.bak. A text box at the bottom right of the second screenshot says 'Use <CTRL> <Space> for content assist'.

	Setup	File
1	Pin Configuration	pins
2	Levels	levels
3	Timing	timing
4	Pattern	all.binl
5	Pin Attributes	all.binl
6	Channel Attributes	all.binl.bak
7	Analog Control	
8	Waveform	
9	Routing	
10	Test Table	

Use <CTRL> <Space> for content assist

Necessary step to make all primary settings (pins/level/timing/pattern) available within the Testflow

3. Element insertion Testsuite

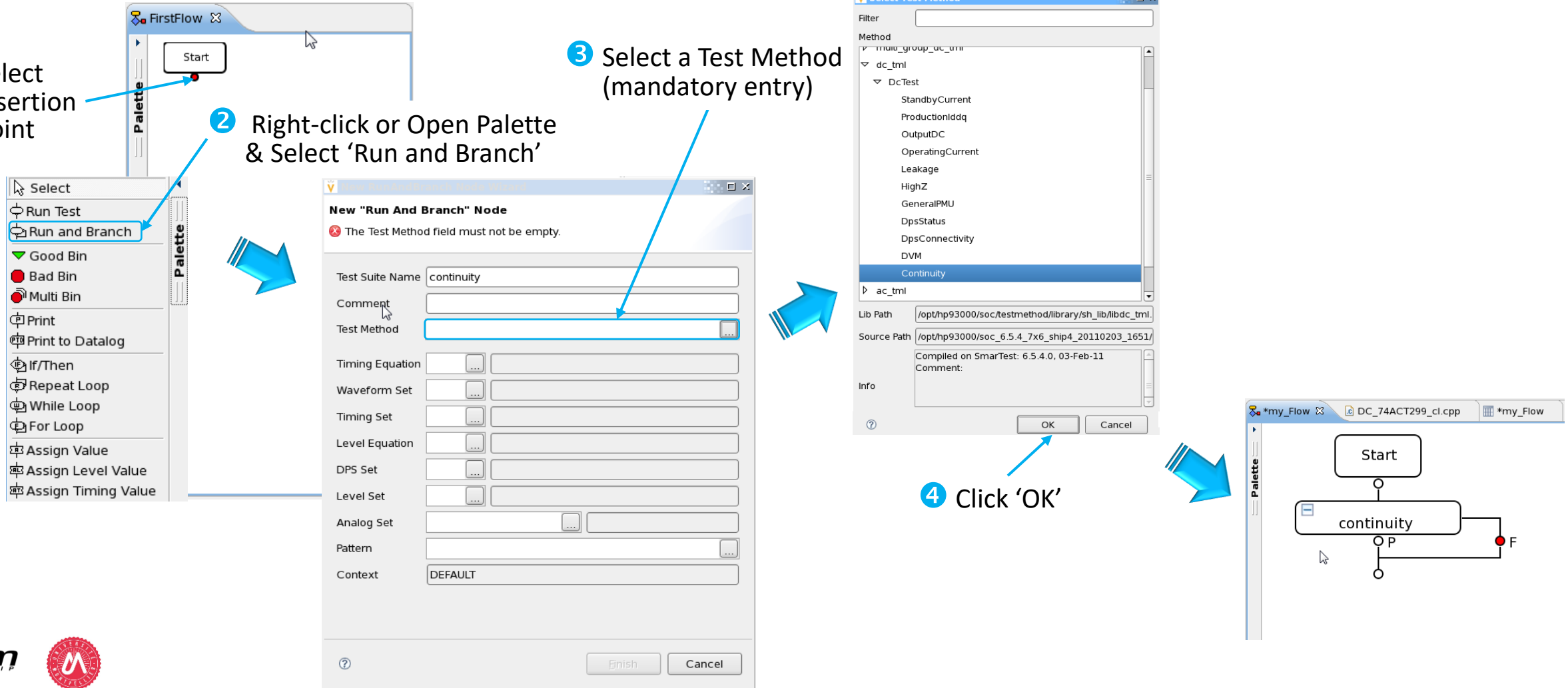
TEST FLOW CREATION IN SMARTTEST

1 Select insertion point

2 Right-click or Open Palette & Select 'Run and Branch'

3 Select a Test Method (mandatory entry)

4 Click 'OK'



3. Element insertion Testsuite

TEST FLOW CREATION IN SMARTTEST

PROPERTIES VIEW

Double-click on
Testsuite will open
the Properties view

Instant Console Properties

type filter text

Property	Value
Test Suite	gross_func
Comment	
Primaries	...
Timing	1, 1, 1
Level	2, 2, 1
Analog	
Pattern	gross_func
Context	DEFAULT
Test Type	M
Test Method	my_ac_classic_tm_project.ClassAcTest.functionalTest
Parameters	
Limits	...
Flags	...
Site Control	...
Results (Site in Focus)	...

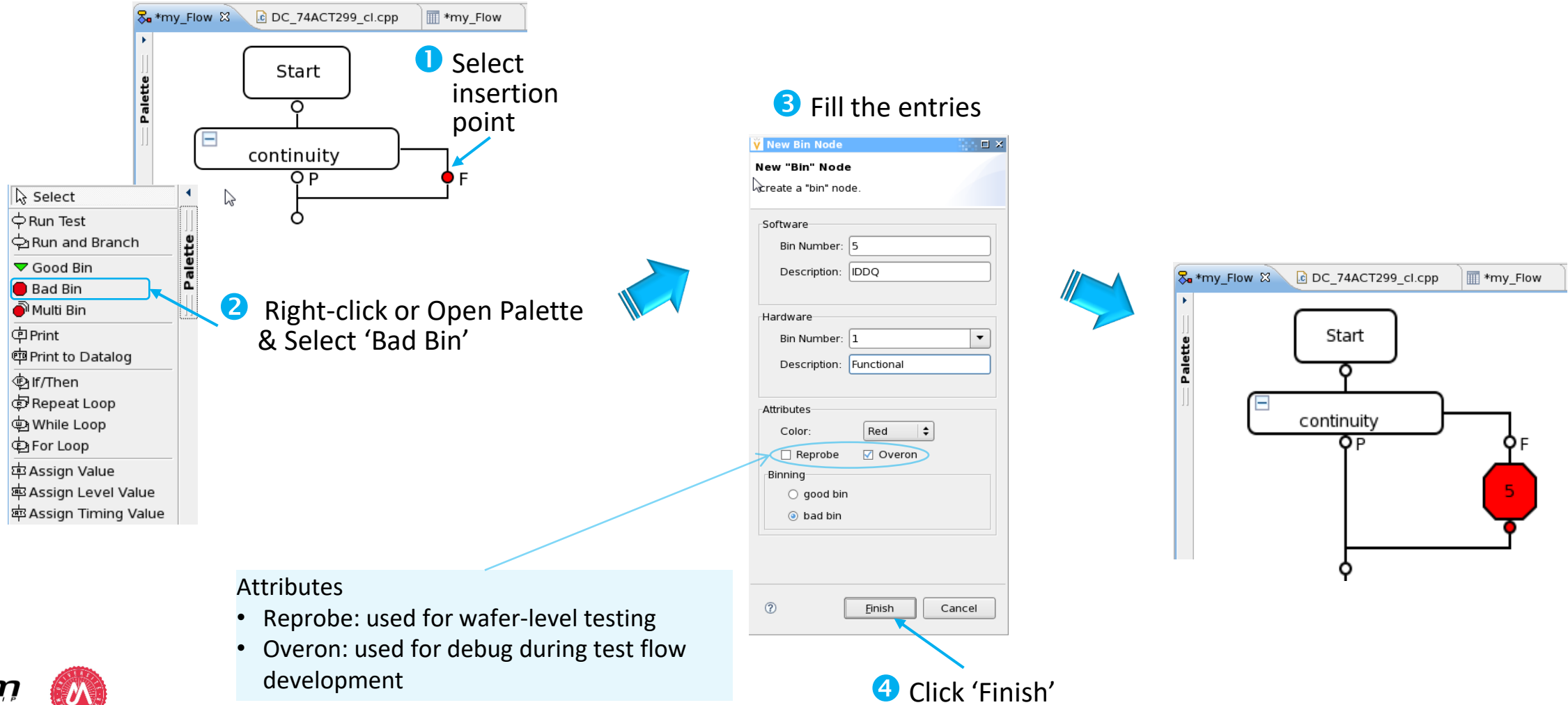
Signal

	CP (PW)	CP (SC)	DS0 (SC)	DS7 (SC)	I/O0 (SC)	I/O1 (SC)	I/O2 (SC)	I/O3 (SC)	I/O4 (SC)	I/O5 (SC)	I/O6 (SC)
X-Mode Area											
Protocol											
Vector#	Instruction	Comment									
0	reset		1	1	0	0	0	0	0	0	0
1	hold		1	1	0	0	X	X	X	X	X
2	par load 0x80		1	1	0	0	1	0	0	0	0
3	shift right		1	1	0	0	L	H	L	L	L
4			1	1	0	0	L	L	H	L	L
5			1	1	0	0	L	L	L	H	L
6			1	1	0	0	L	L	L	L	H
7			1	1	0	0	L	L	L	L	H
8			1	1	0	0	L	L	L	L	H
9			1	1	0	0	L	L	L	L	L
10			1	1	0	0	L	L	L	L	L
11			1	1	0	1	L	L	L	L	L
12			1	1	0	1	L	L	L	L	H

Selecting value and pressing "F3" will open associated editor (e.g. vector editor will open when a pattern label is selected)

3. Element insertion Bin

TEST FLOW CREATION IN SMARTTEST

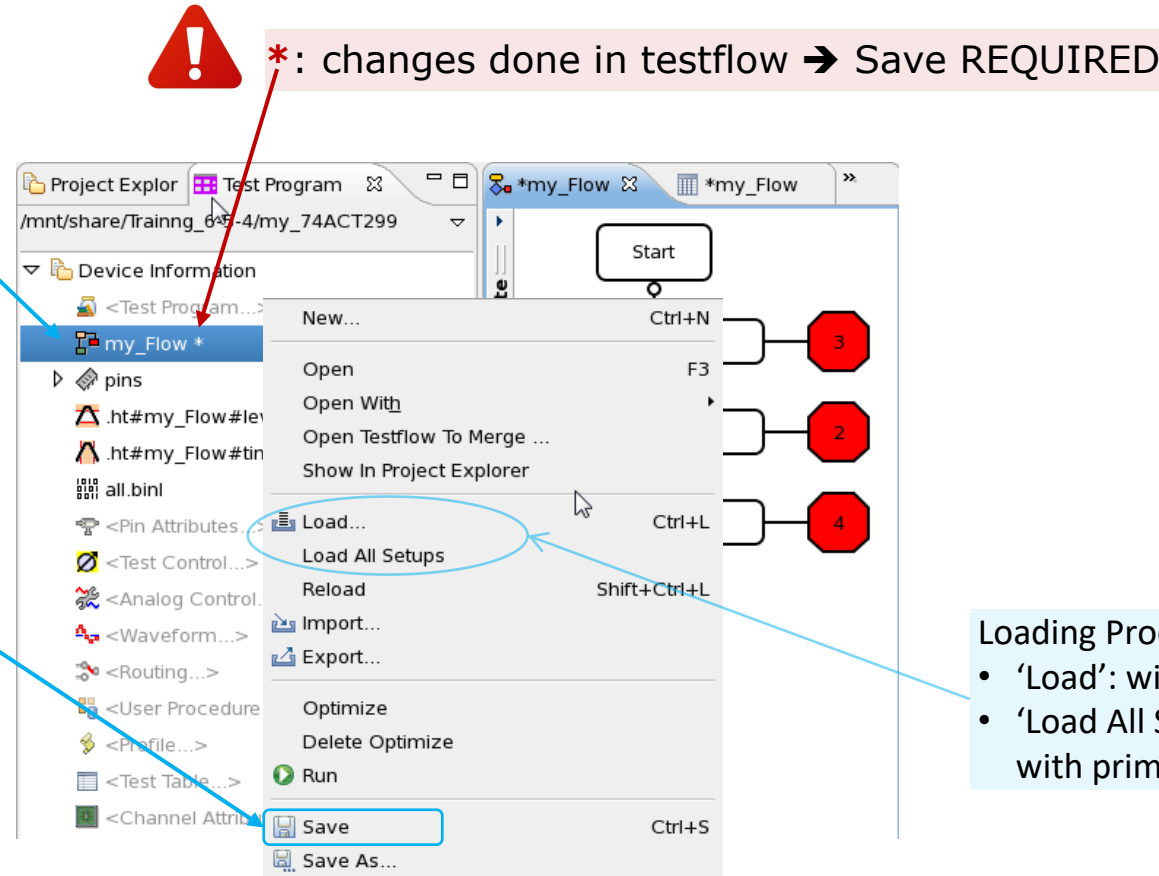


4. Save testflow

TEST FLOW CREATION IN SMARTTEST

1 Right-click on testflow item in Test Program Explorer

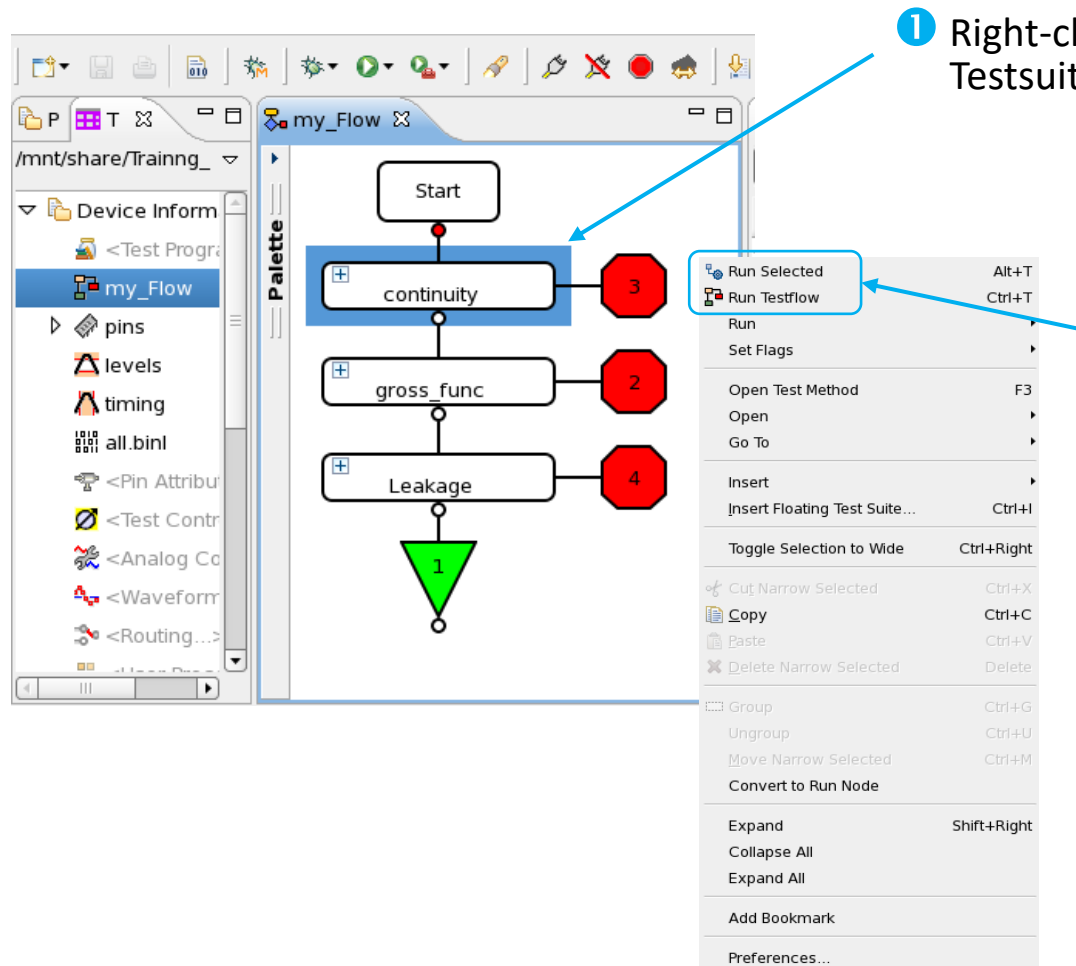
2 Select 'Save'



Loading Process in two steps

- 'Load': will open 'Select file to load'
- 'Load All Setups': will fill tester-hardware with primary data

TEST FLOW EXECUTION IN SMARTTEST



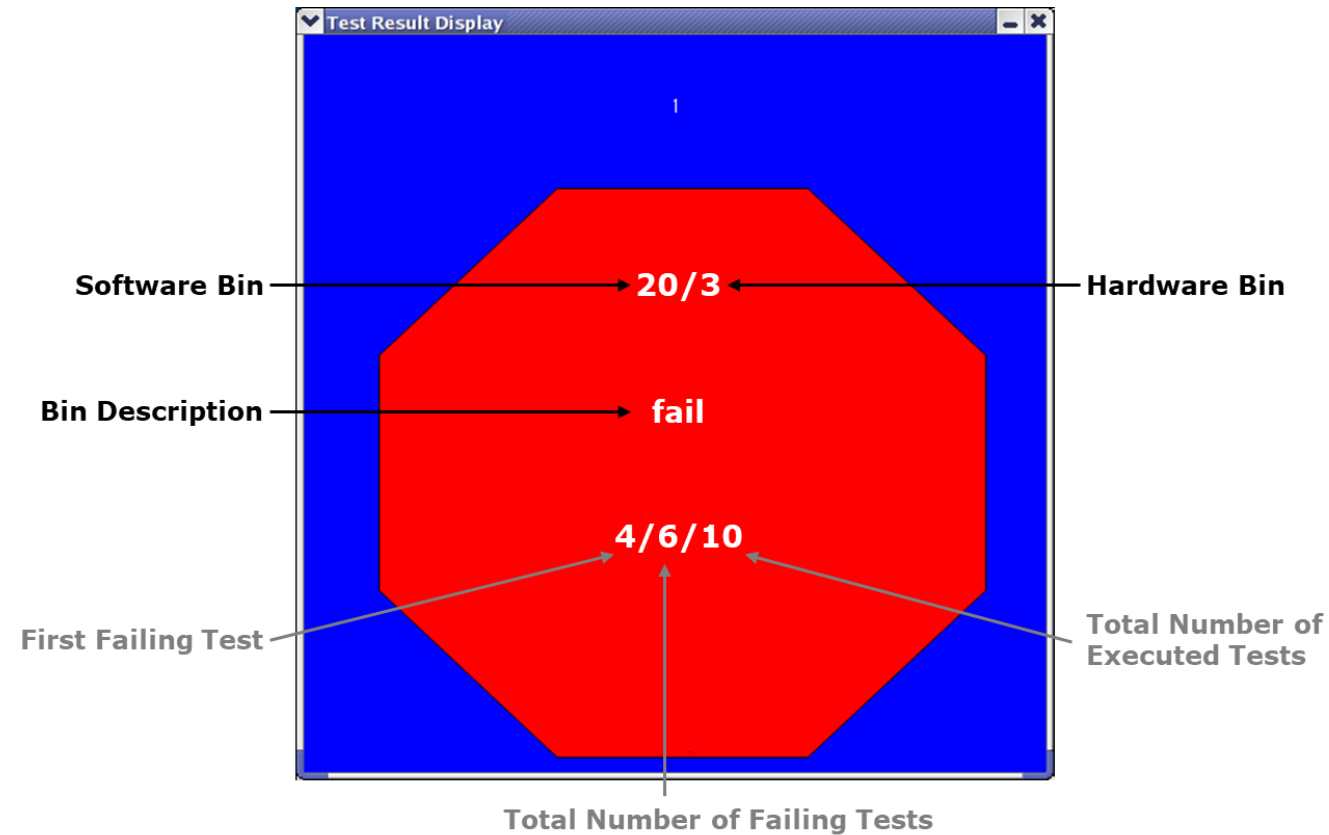
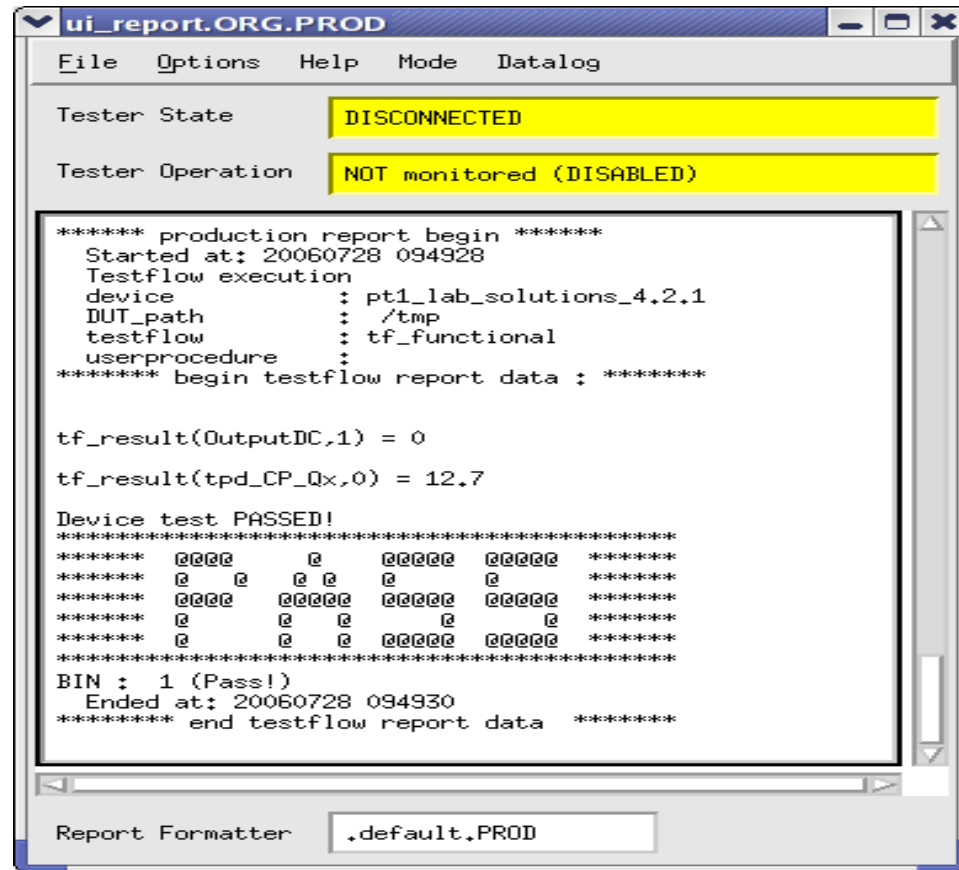
The screenshot displays the SmartTest software interface. On the left, a file explorer shows the project structure, including a folder named 'my_Flow'. The main workspace shows a test flow diagram with nodes: 'Start', 'continuity', 'gross_func', 'Leakage', and a green triangle labeled '1'. A right-click context menu is open over the 'continuity' node, which is highlighted with a blue border. The menu options include 'Run Selected' (Alt+T), 'Run Testflow' (Ctrl+T), 'Run', 'Set Flags', 'Open Test Method' (F3), 'Open', 'Go To', 'Insert', 'Insert Floating Test Suite...' (Ctrl+I), 'Toggle Selection to Wide' (Ctrl+Right), 'Cut Narrow Selected' (Ctrl+X), 'Copy' (Ctrl+C), 'Paste' (Ctrl+V), 'Delete Narrow Selected' (Delete), 'Group' (Ctrl+G), 'Ungroup' (Ctrl+U), 'Move Narrow Selected' (Ctrl+M), 'Convert to Run Node', 'Expand' (Shift+Right), 'Collapse All', 'Expand All', 'Add Bookmark', and 'Preferences...'. Two blue arrows point to the 'Run Selected' and 'Run Testflow' options, corresponding to the numbered instructions.

1 Right-click on a Testsuite

2 Choose

- 'Run Selected': single Testsuite execution
- 'Run Testflow': overall Testflow execution

TEST FLOW EXECUTION IN SMARTTEST

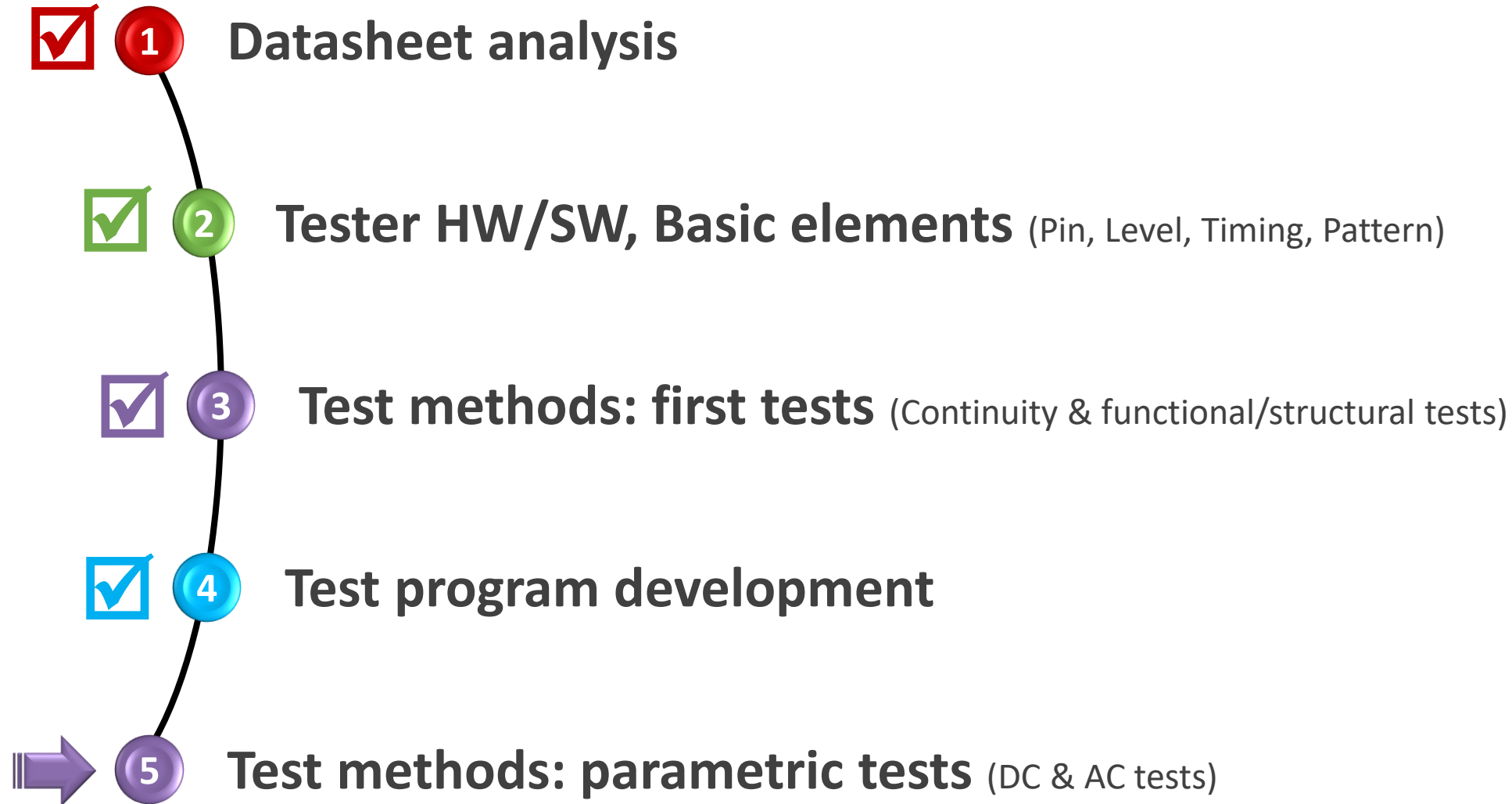




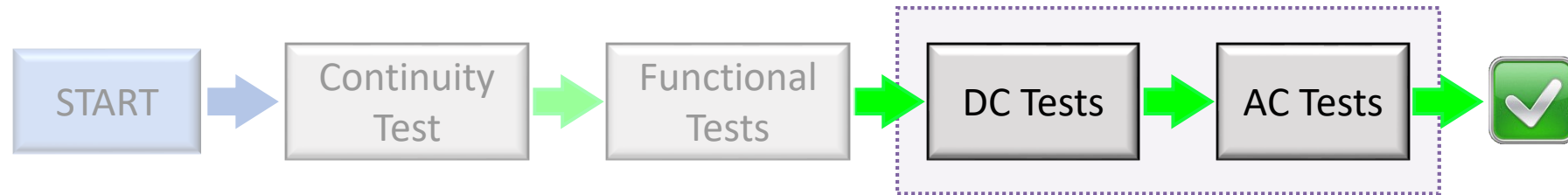
Lab & Exercises:

74ACT299 Test Program Development: First Test Flow *(off-line + on-line)*

LEARNING STEPS

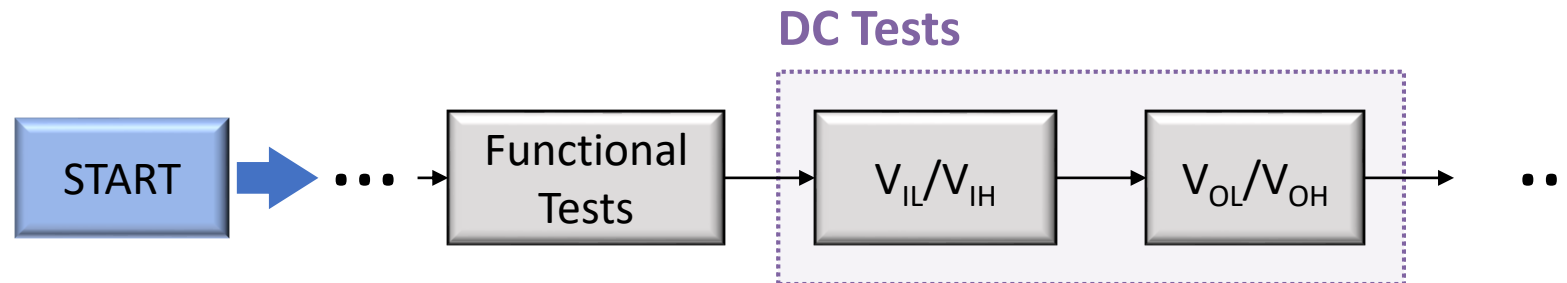


- Production Test Flow



DC TESTS

- Purpose
 - Verify device DC performances, once functionality is OK
- Classical Tests
 - V_{IL}/V_{IH} , V_{OL}/V_{OH}

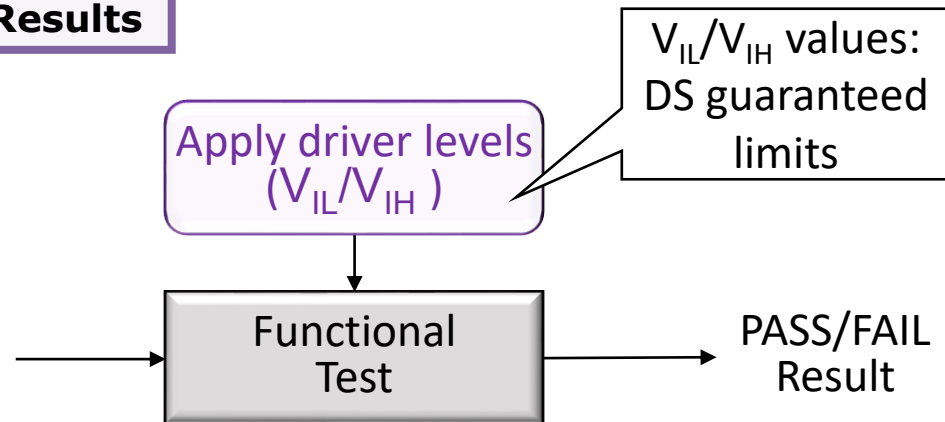


Can be based on functional tests or on V/I measurements

V_{IL}/V_{IH} TEST

- Purpose
 - Ensure that the input pins can correctly sense the proper logic levels when programmed V_{IL}/V_{IH} voltages are applied
- Principle
 - Functional test with driver levels configured at datasheet V_{IL}/V_{IH} values for input pins
(relaxed constraints on comparator levels for output pins)

Pass/Fail Results



DC Electrical Characteristics for ACT

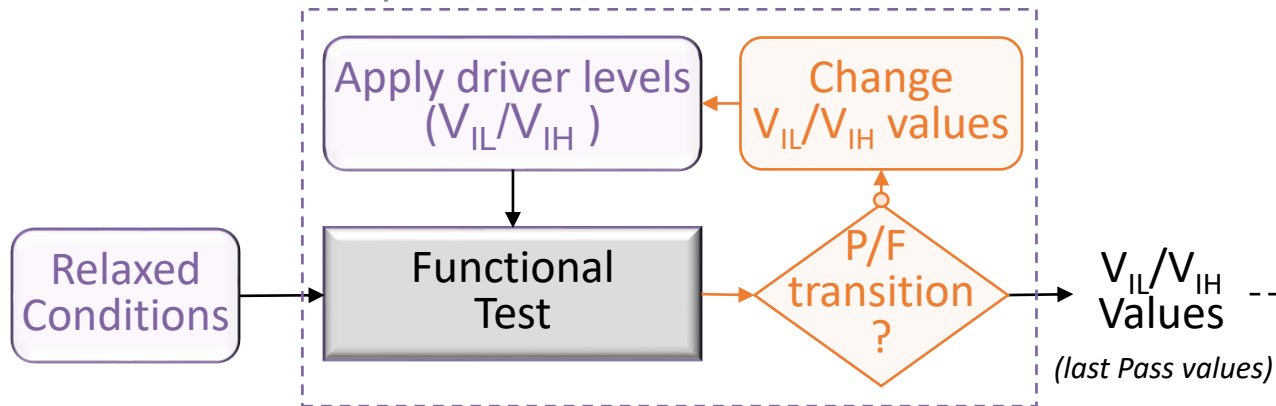
Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{IL}	Maximum LOW Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8		V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$

V_{IL}/V_{IH} TEST

- Purpose
 - Ensure that the input pins can correctly sense the proper logic levels when programmed V_{IL}/V_{IH} voltages are applied
- Principle
 - Iterations of functional test with changing of V_{IL}/V_{IH} values for input pins
(relaxed constraints on comparator levels for output pins)

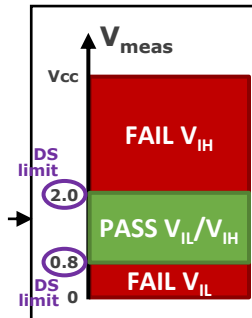
Meas. Values

Loop: Search for value corresponding to P/F transition in functional test



DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = 25 °C		T _A = -40 °C to +85 °C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
V _{IL}	Maximum LOW Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8		V	V _{OUT} = 0.1V or V _{CC} - 0.1V

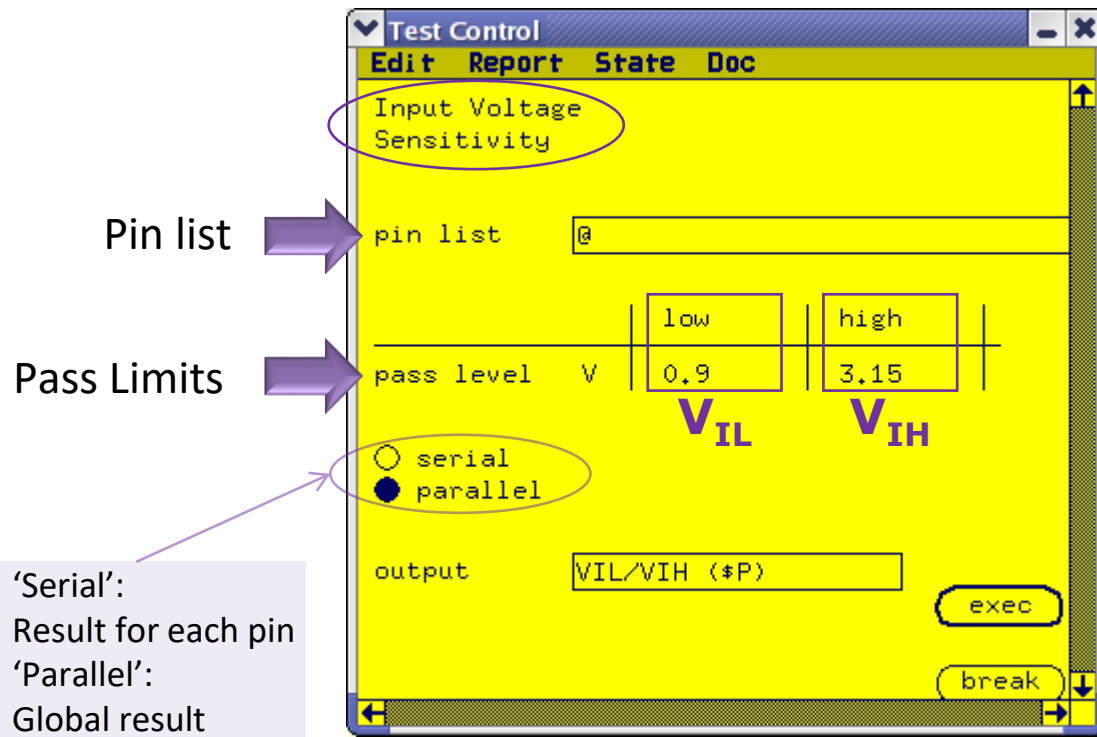


V_{IL}/V_{IH} Test Result

- PASS if $V_{IL-meas} \geq V_{IL-limit}$ & $V_{IH-meas} \leq V_{IH-limit}$
- FAIL otherwise

V_{IL}/V_{IH} TEST IN SMARTTEST

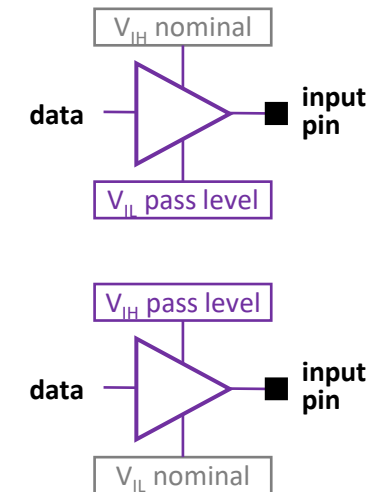
Test Function: 'Input Voltage Sensitivity'



- 'Serial':
Result for each pin
- 'Parallel':
Global result
for the pin list

Test Procedure

1. Set V_{IL} to low pass level
Execute functional test
2. Set V_{IH} to high pass level
Set back V_{IL} to nominal level
Execute functional test



3. Return FAIL if either execution fails, otherwise return PASS

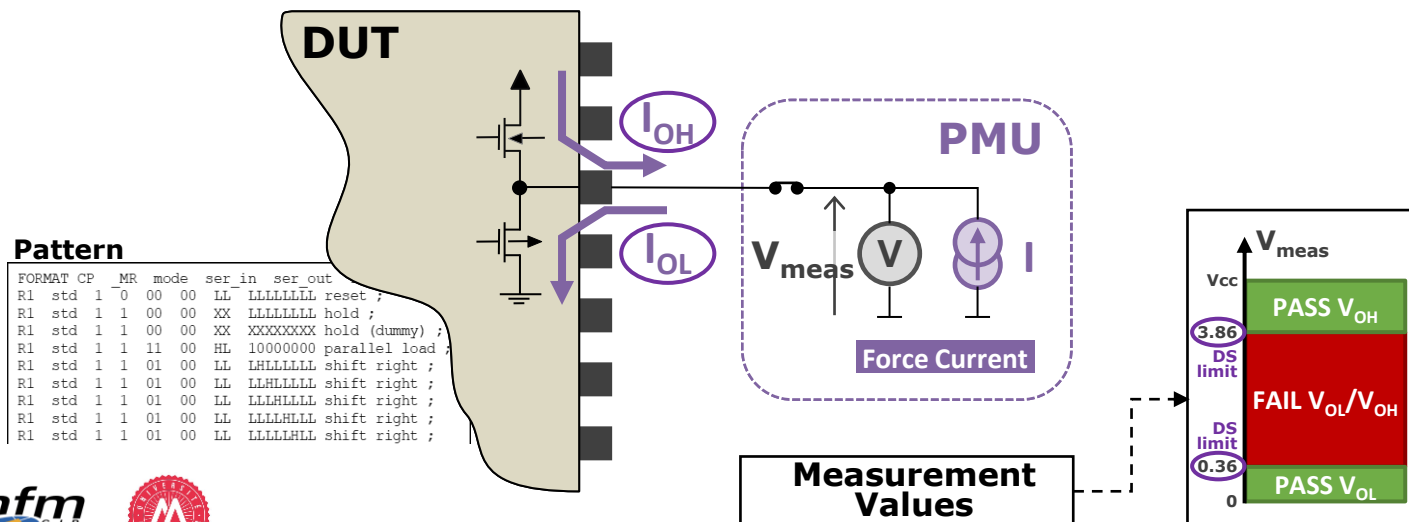
* V_{IL}/V_{IH} measurement: iterations of steps 1 & 2 with incremental change of V_{IL}/V_{IH} setting to identify P/F transition (meas. value = last Pass value)
Return FAIL if measured $V_{IL} < \text{low pass level}$ or measured $V_{IH} > \text{high pass level}$, otherwise return PASS

TEST METHODS: DC PARAMETRIC TESTS

V_{OL}/V_{OH} TEST

- Purpose
 - Verify voltage/current capabilities: ensure that the V_{OL}/V_{OH} voltages are not too much degraded while output pins deliver the specified I_{OL}/I_{OH} current
- Principle
 - Force I_{OL}/I_{OH} current on output pins and measure the corresponding V_{OL}/V_{OH} voltage

Implementation with PMU



DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = 25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4		V	I _{OUT} = -50 μA
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.0001	3.86	3.76		V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 5)
		5.5	0.001	4.86	4.76		V	I _{OH} = -24 mA (Note 5)
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 5)
		5.5	0.001	0.1	0.1		V	I _{OL} = 24 mA (Note 5)

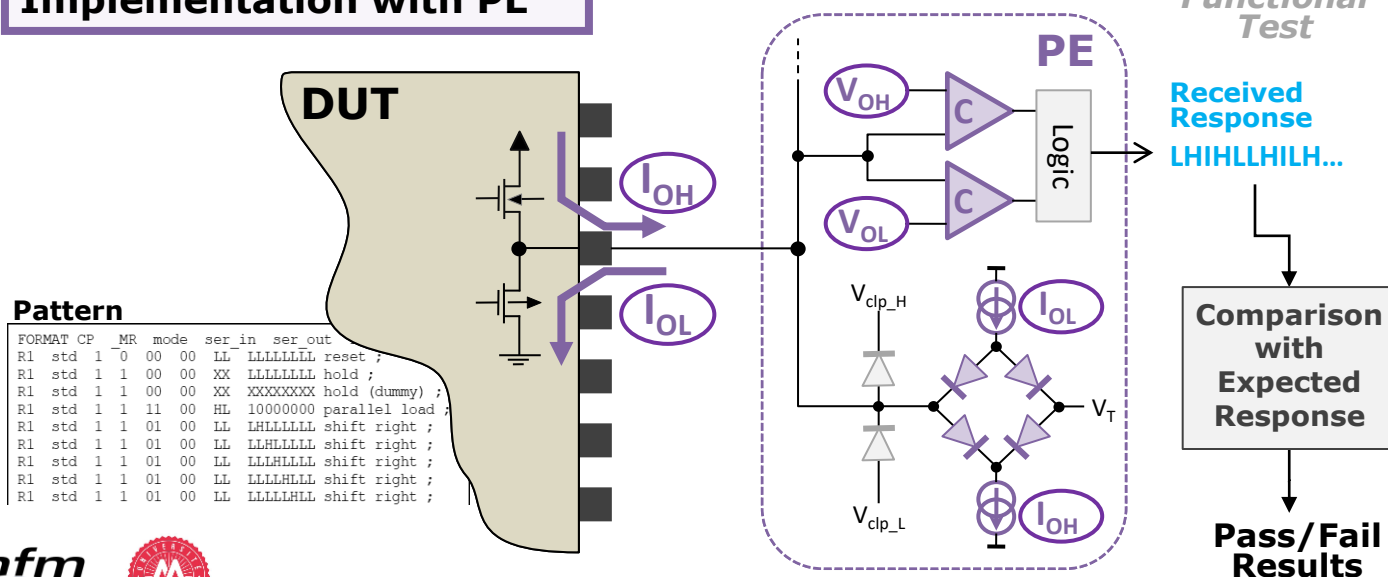
V_{OL}/V_{OH} Test Result

- PASS if $V_{OL-meas} \leq V_{OL-limit}$ & $V_{OH-meas} \geq V_{OH-limit}$
- FAIL otherwise

V_{OL}/V_{OH} TEST

- Purpose
 - Verify voltage/current capabilities: ensure that the V_{OL}/V_{OH} voltages are not too much degraded while output pins deliver the specified I_{OL}/I_{OH} current
- Principle
 - Force I_{OL}/I_{OH} current on output pins and measure the corresponding V_{OL}/V_{OH} voltage

Implementation with PL



DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = 25° C		T _A = -40° C to +85° C		Units	Conditions
			Typ	Guaranteed Limits				
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	0.0001	3.86	3.76	V		V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA
		5.5		4.86	4.76	I _{OH} = -24 mA (Note 5)		
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V		V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA
		5.5		0.36	0.44	I _{OL} = 24 mA (Note 5)		

If measurement values are demanded:

- Iterations of functional test to identify P/F transition (meas. values = last Pass values)
- Comparison of meas. values with V_{OL}/V_{OH} limits to return a Pass/Fail result

V_{OL}/V_{OH} TEST IN SMARTTEST

Test Function:
'Output DC'

I_{OL}/V_{OL}

I_{OH}/V_{OH}

Pin list

The screenshot shows the 'Test Control' window with the 'Output DC' test function selected. The 'pin list' is set to 'ser_out'. The 'force current' table shows 'low' at 6 mA and 'high' at -6 mA. The 'pass max/min' table shows 'low' at 0.8 V and 'high' at 3.8 V. The 'Additional PMU parameters' table shows 'SPMU clamp voltage' at -0.1 V and 'settling time' at 1 ms. The 'Instrument' section has 'PPMU' selected. The 'vec. range' is set to '10 - 20' and the 'output' is 'Vout (\$P)'.

	unit	low	high
force current	mA	6	-6
pass max/min	V	0.8	3.8

	V	ms
SPMU clamp voltage	-0.1	
settling time		1

Additional PMU parameters

- ☒ PPMU
- ☐ PPMU/term
- ☐ Programable Load
- ☐ SPMU
- ☐ SPMU/term

vec. range: 10 - 20

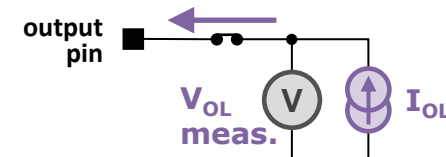
output: Vout (\$P)

Instrument

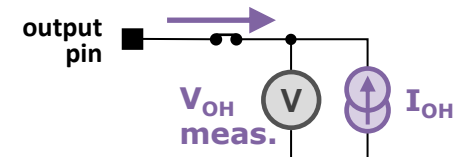
Test Procedure with PMU option

1. Execute test vectors; Scan for 'L' or 'H' state in a pin-by-pin basis
2. For first pin & for each vector: Connect PMU, Force Current@spec value & Measure Voltage

'L' state expected



'H' state expected



3. Repeat for remaining pins
4. Compare to pass values

V_{OL}/V_{OH} TEST IN SMARTTEST

Test Function:
'Output DC'

I_{OL}/V_{OL}

I_{OH}/V_{OH}

Test Procedure with PMU option

1. Execute test vectors; Scan for 'L' or 'H' state in a pin-by-pin basis in the specified vector range



Make sure that both 'L' & 'H' states are present in the specified vector range for the pins under test

```

FORMAT CP  _MR mode ser_in ser_out io_pins ;
R1 std 1 0 00 00 LL LLLLLLLL reset ;
R1 std 1 1 00 00 XX LLLLLLLL hold ;
R1 std 1 1 00 00 XX XXXXXXXX hold (dummy) ;
R1 std 1 1 11 00 HL 10000000 parallel load ;
R1 std 1 1 01 00 LL LHLLLLLL shift right ;
R1 std 1 1 01 00 LL LHLLLLLL shift right ;
R1 std 1 1 01 00 LL LLLHLLLL shift right ;
R1 std 1 1 01 00 LL LLLLHLLL shift right ;
R1 std 1 1 01 00 LL LLLLHLLL shift right ;
R1 std 1 1 01 00 LL LLLLHLLL shift right ;
R1 std 1 1 01 00 LL LLLLHLLL shift right ;
R1 std 1 1 01 00 LH LLLLHLLL shift right ;
R1 std 1 1 01 00 LL LLLLHLLL shift right ;
R1 std 1 1 10 01 LH LLLLHLLL shift in left ;
R1 std 1 1 10 01 LH LLLLHLLL shift in left ;
R1 std 1 1 10 00 LL LLLLHLLL shift left ;
R1 std 1 1 10 00 LL LLLLHLLL shift left ;
R1 std 1 1 10 00 LL LLLLHLLL shift left ;
R1 std 1 1 10 00 LL LLLLHLLL shift left ;
R1 std 1 1 10 00 LL LLLLHLLL shift left ;
R1 std 1 1 10 00 LH LLLLHLLL shift left ;
R1 std 1 1 10 00 HL HLLLHLLL shift left ;
R1 std 1 1 10 00 HL HLLLHLLL shift left ;
R10 std 1 1 00 00 XX HLLLLLLL hold ;
  
```

Pin list

Instrument

The screenshot shows the 'Test Control' window with the 'Edit' tab selected. The 'Output DC' test function is chosen. The 'pin list' field contains 'ser_out'. The 'force current' table shows 'mA' with 'low' at 6 and 'high' at -6, and 'pass max/min' with 'V' at 0.8 and 3.8. The 'Additional PMU parameters' table shows 'SPMU clamp voltage' with 'V' at -0.1 and 1, and 'settling time' with 'ms' at 1. The 'Instrument' section has radio buttons for PPMU, PPMU/term, Programable Load, SPMU, and SPMU/term, with PPMU selected. The 'vec. range' is set to '10 - 20' and the 'output' is 'Vout (\$P)'. A note 'DC measurements @ specified vectors' points to the vector range field.

V_{OL}/V_{OH} TEST IN SMARTTEST

Test Function:
'Output DC'

I_{OL}/V_{OL}

I_{OH}/V_{OH}

Pin list

	unit	low	high
force current	mA	6	-6
pass max/min	V	0.8	3.8

	V	
SPMU clamp voltage	-0.1	
pass min/max		
settling time	ms	1

Instrument selection:

- ☒ PPMU
- ☐ PPMU/term
- ☒ Programable Load
- ☐ SPMU
- ☐ SPMU/term

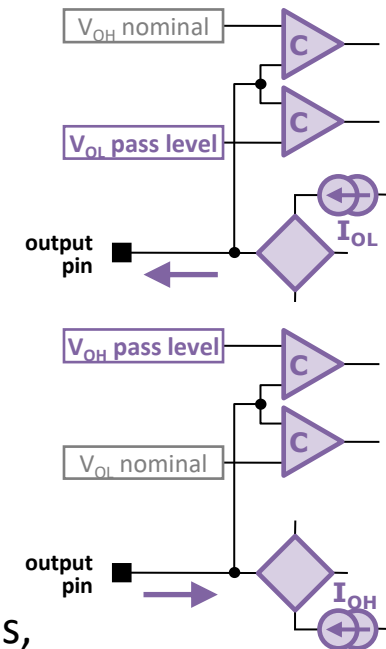
vec. range: 10 - 20

output: Vout (\$P)

Instrument

Test Procedure with PL option

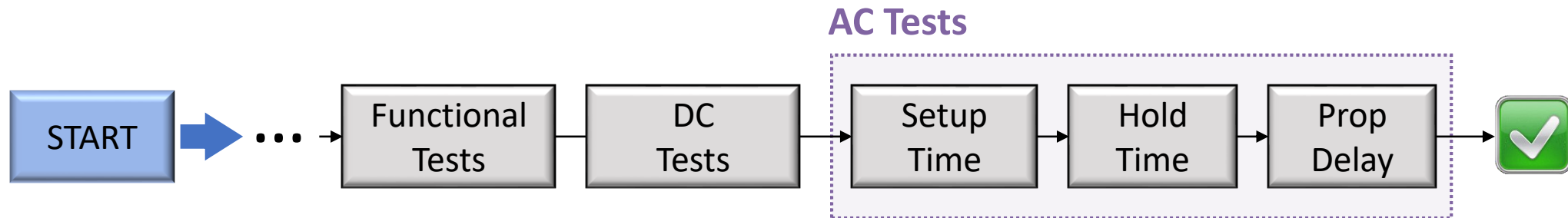
1. Set V_{OL} to low pass level
Set active load to I_{OL}
Execute functional test
2. Set back V_{OL} to nominal level
Set V_{OH} to high pass level
Set active load to I_{OH}
Execute functional test
3. Return FAIL if either execution fails, otherwise return PASS



* V_{OL}/V_{OH} measurement: iterations of steps 1 & 2 with incremental change of V_{OL}/V_{OH} setting to identify P/F transition (meas. value = last Pass value); Return FAIL if measured $V_{OL} >$ low pass level or measured $V_{OH} <$ high pass level, otherwise return PASS

AC TESTS

- Purpose
 - Verify device AC performances, once functionality & DC performances are OK
- Classical Tests
 - Setup & hold times (inputs), propagation delay (outputs), frequency

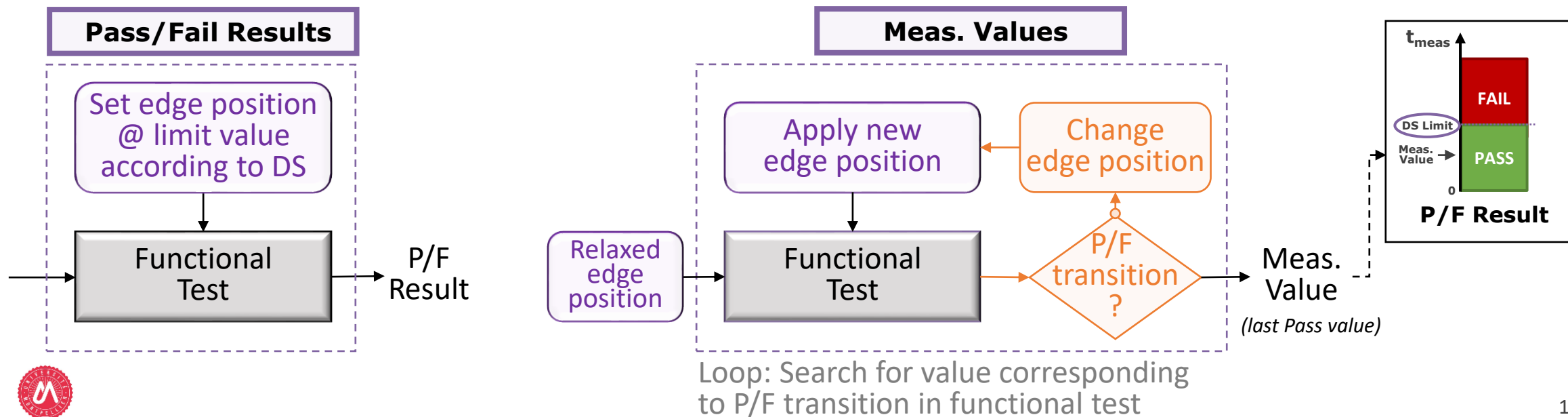


All AC tests are based on functional tests

AC TESTS

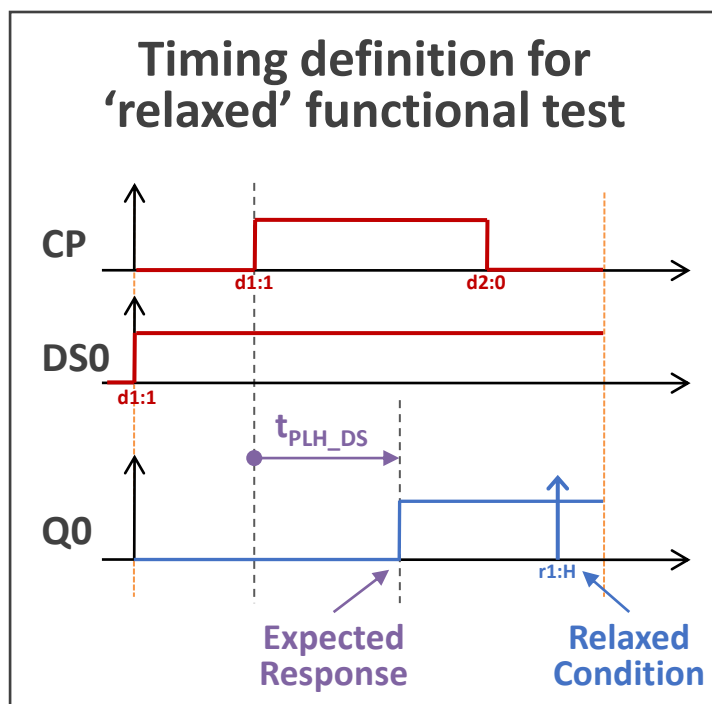
• Principle

- Pass/Fail Results: one functional test performed with edge position set at limit value w.r.t. datasheet specification for the targeted performance
- Measurement Values: iterations of functional test with changing of edge position in order to identify Pass/Fail transition (meas. value = last Pass value); Comparison of meas. value with datasheet specification to return a Pass/Fail result



AC TESTS

- Illustration: t_{PLH}



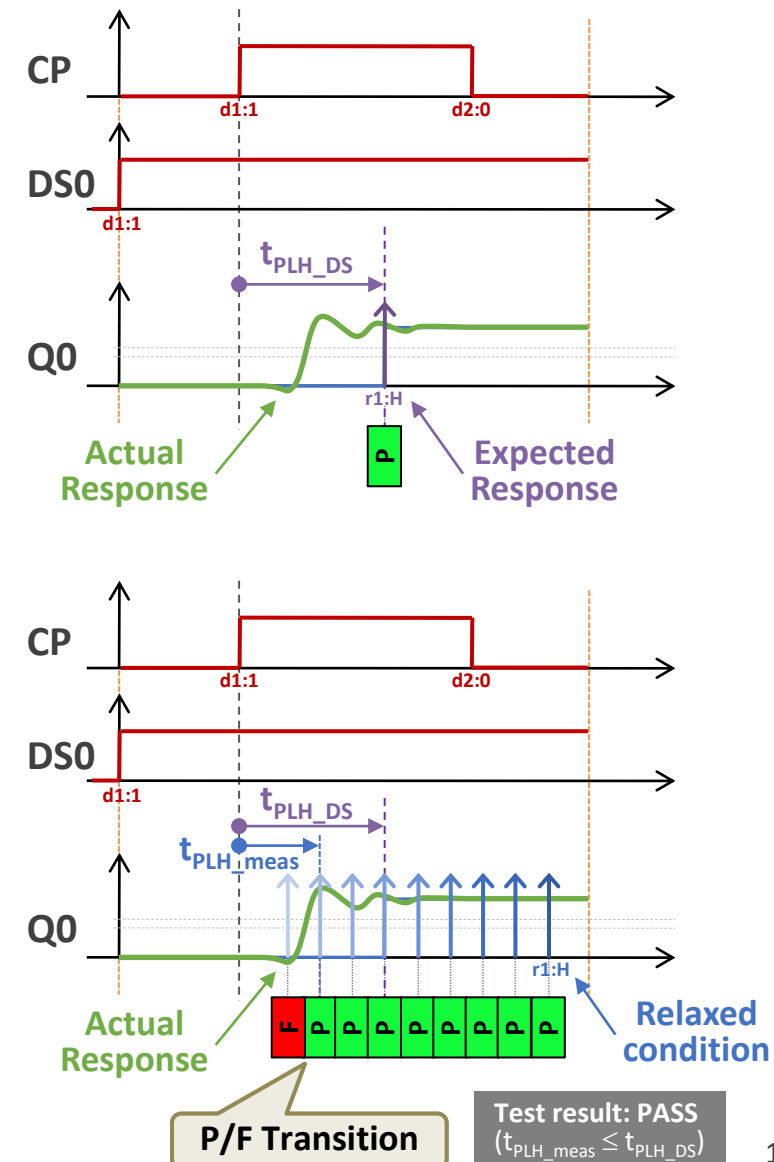
One functional test

Pass/Fail Result

Iterations of functional test

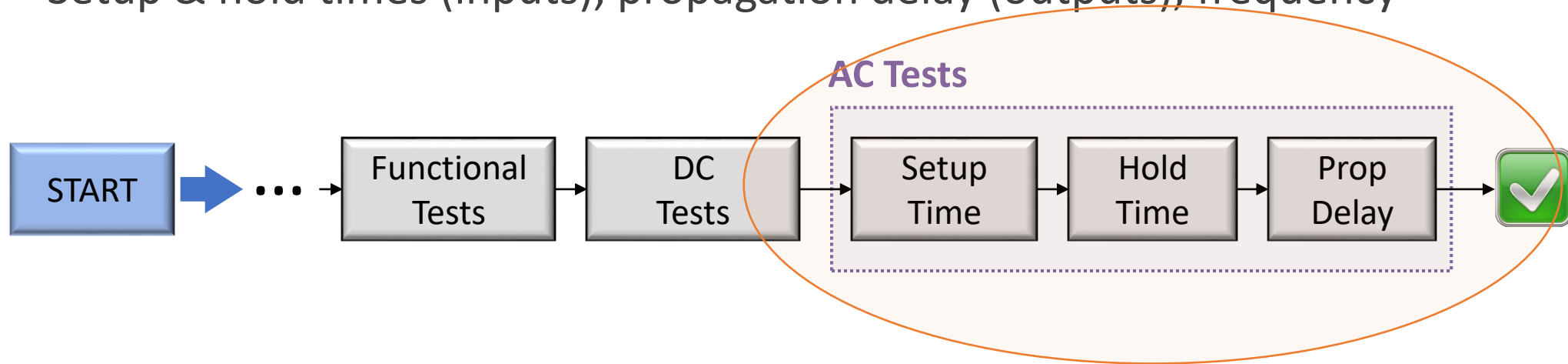
Meas. Value
(last Pass value)

PROP DELAY TEST



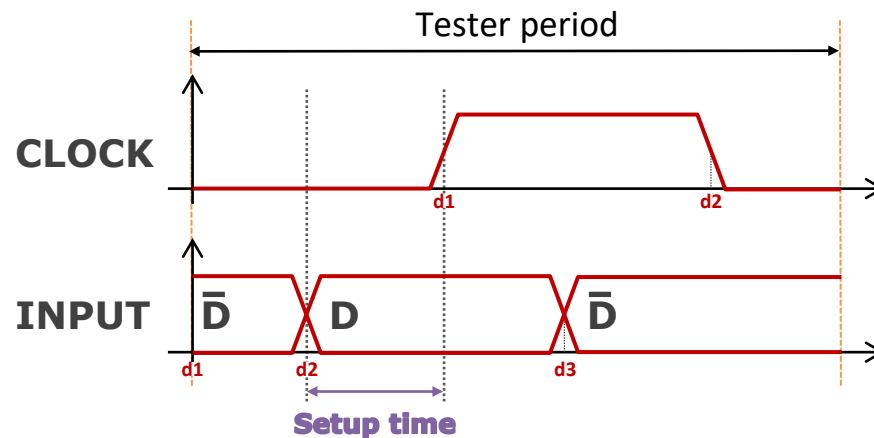
AC TESTS

- Purpose
 - Verify device AC performances, once functionality & DC performances are OK
- Classical Tests
 - Setup & hold times (inputs), propagation delay (outputs), frequency



SETUP TIME TEST

- Definition
 - Minimum amount of time the data input must be held steady before the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(3 edges with SBC format to handle both setup
& hold times)

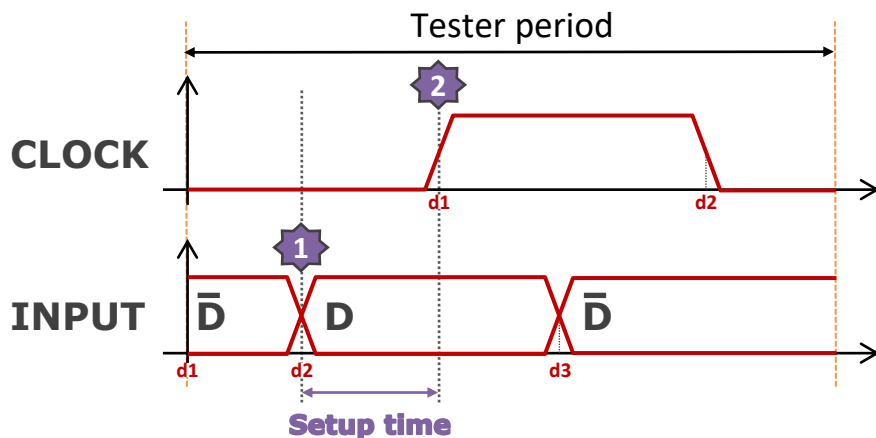
AC Operating Requirements for ACT

Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum			
t _S	Setup Time, HIGH or LOW S _n or S ₁ to CP	5.0	2.0	5.0	5.5		ns
t _H	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	-2.0	1.0	1.0		ns
t _S	Setup Time, HIGH or LOW I/O _n to CP	5.0	1.5	4.0	4.5		ns
t _H	Hold Time, HIGH or LOW I/O _n to CP	5.0	-1.0	1.0	1.0		ns
t _S	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	1.5	4.5	5.0		ns
t _H	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	-1.0	1.0	1.0		ns
t _W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5		ns
t _W	MR Pulse Width, LOW	5.0	2.0	3.5	3.5		ns
t _{REC}	Recovery Time, MR to CP	5.0	0	1.5	1.5		ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

SETUP TIME TEST IN SMARTTEST

- Definition
 - Minimum amount of time the data input must be held steady before the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(3 edges with SBC format to handle both setup
& hold times)

Test Function: 'Setup Time'

Pin list

- 1 Edge under focus
- 2 Reference (optional)

edge/param devcyc	d2	
[ref. pin/time]	LE	CP
[ref. devcyc]		
pass setup time	ns	5

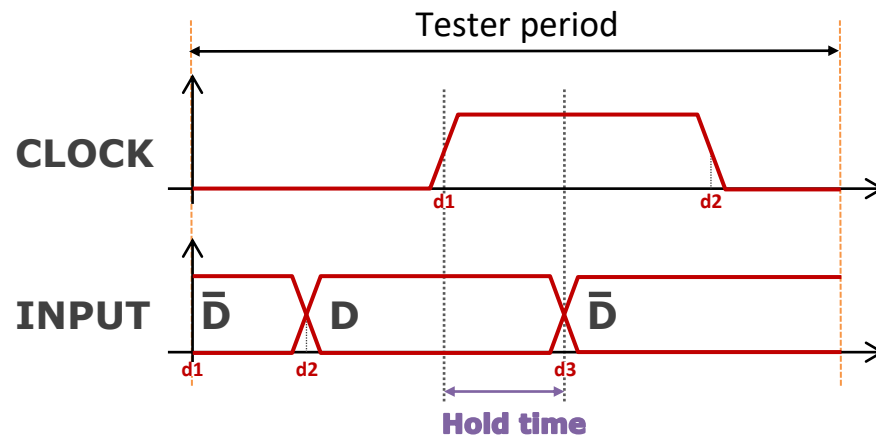
Limit Value

serial
parallel

output: tsu (\$P)

HOLD TIME TEST

- Definition
 - Minimum amount of time the data input must be held steady after the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(3 edges with SBC format to handle both setup
& hold times)

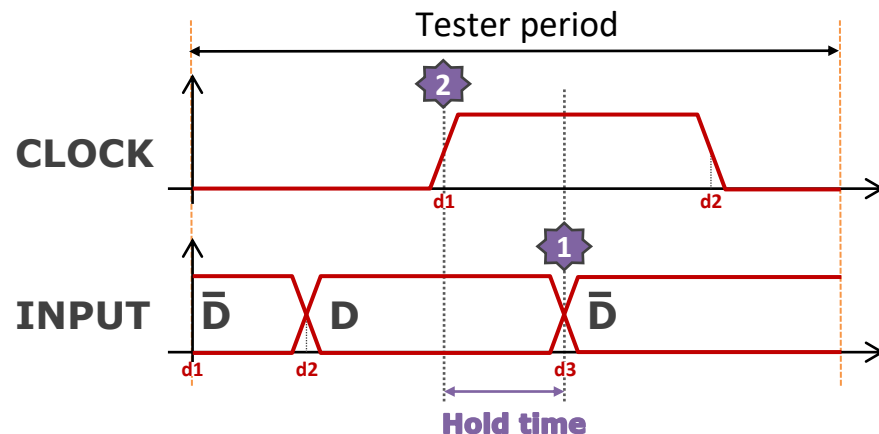
AC Operating Requirements for ACT

Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum			
t ₀	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.5	ns	
t _H	Hold Time, HIGH or LOW S _n or S ₁ to CP	5.0	-2.0	1.0	1.0	ns	
t ₀	Setup Time, HIGH or LOW I/O _n to CP	5.0	1.5	4.0	4.5	ns	
t _H	Hold Time, HIGH or LOW I/O _n to CP	5.0	-1.0	1.0	1.0	ns	
t ₀	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	1.5	4.5	5.0	ns	
t _H	Hold Time, HIGH or LOW DS _n or DS ₇ to CP	5.0	-1.0	1.0	1.0	ns	
t _W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns	
t _W	MR Pulse Width, LOW	5.0	2.0	3.5	3.5	ns	
t _{REC}	Recovery Time, MR to CP	5.0	0	1.5	1.5	ns	

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

HOLD TIME TEST IN SMARTTEST

- Definition
 - Minimum amount of time the data input must be held steady after the transition of a reference signal (clock)
- Test performed on input pins only



Appropriate WF definition required
(3 edges with SBC format to handle both setup & hold times)

Test Function: 'Hold Time'

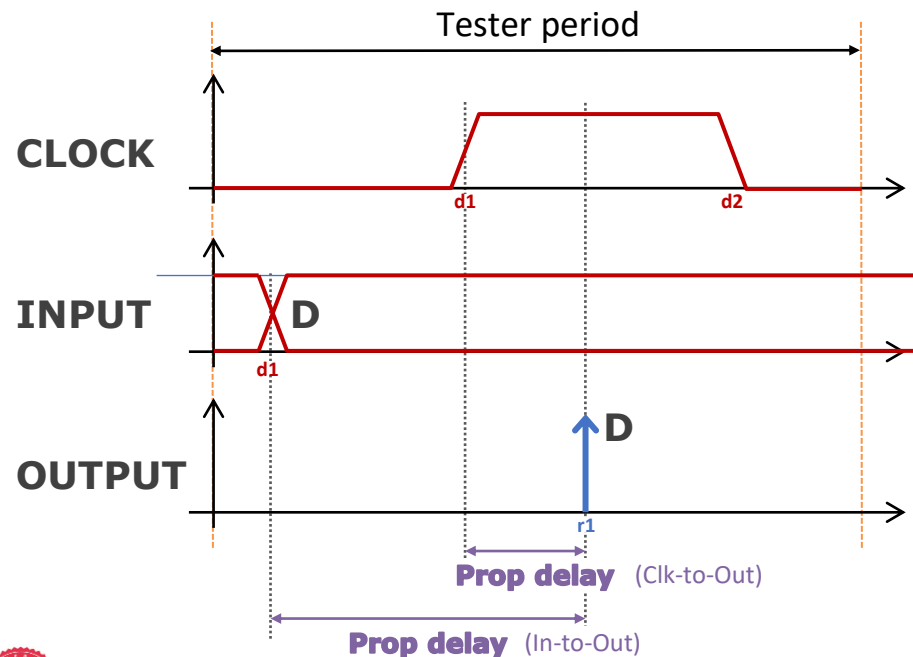
Pin list

- 1 Edge under focus
- 2 Reference (optional)

The screenshot shows the **Test Control** window for the **Hold Time** test function. The window has a yellow background and a blue title bar. The **Pin list** is set to **DS0,DS7**. The **edge/param** is set to **devcyc d3**. The **[ref. pin/time]** is set to **LE CP**. The **[ref. devcyc]** is set to **ns**. The **pass hold time** is set to **ns**. The **output** is set to **thd (#P)**. A **Limit Value** is indicated by a circled '1'.

PROPAGATION DELAY TEST

- Definition
 - Maximum amount of time that ensures the presence of the data after a transition of a reference signal (input or clock)
- Test performed on output pins only



AC Electrical Characteristics for ACT

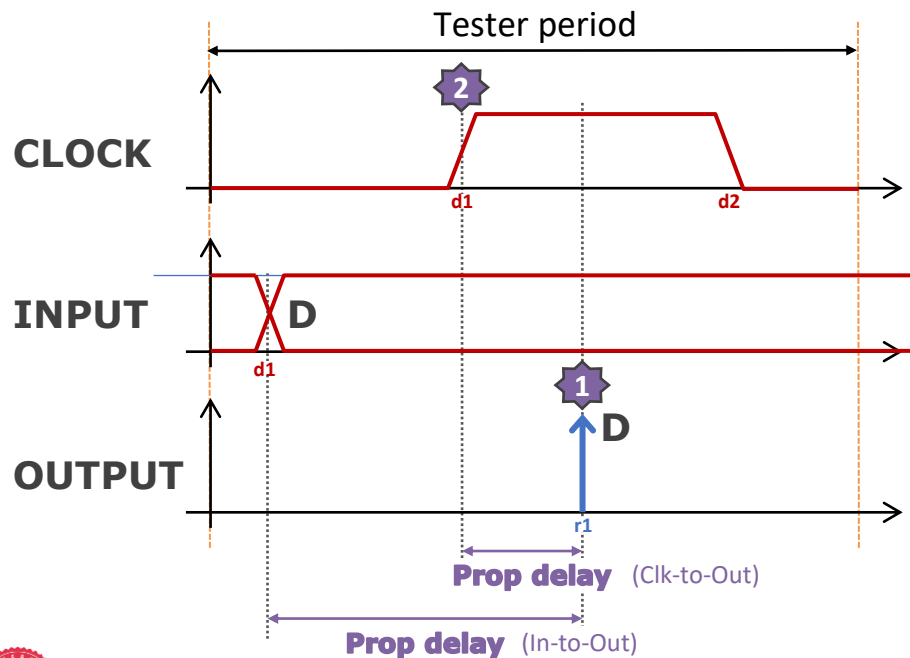
Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t _{PLH}	Propagation Delay CP to I/O _n	5.0	4.5	8.5	12.5	4.5	13.5	ns
t _{PHL}	Propagation Delay CP to I/O _n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t _{PLH}	Propagation Delay MR to Q ₀ or Q ₇	5.0	4.0	14.0	15.0	4.0	18.0	ns
t _{PHL}	Propagation Delay MR to I/O _n	5.0	4.0	13.0	14.5	3.5	17.5	ns



t_{PLH} & t_{PHL} might be different

PROPAGATION DELAY TEST IN SMARTTEST

- Definition
 - Maximum amount of time that ensures the presence of the data after a transition of a reference signal (input or clock)
- Test performed on output pins only



- 1 Edge under focus
- 2 Reference (optional)

Test Function: 'Prop Delay'

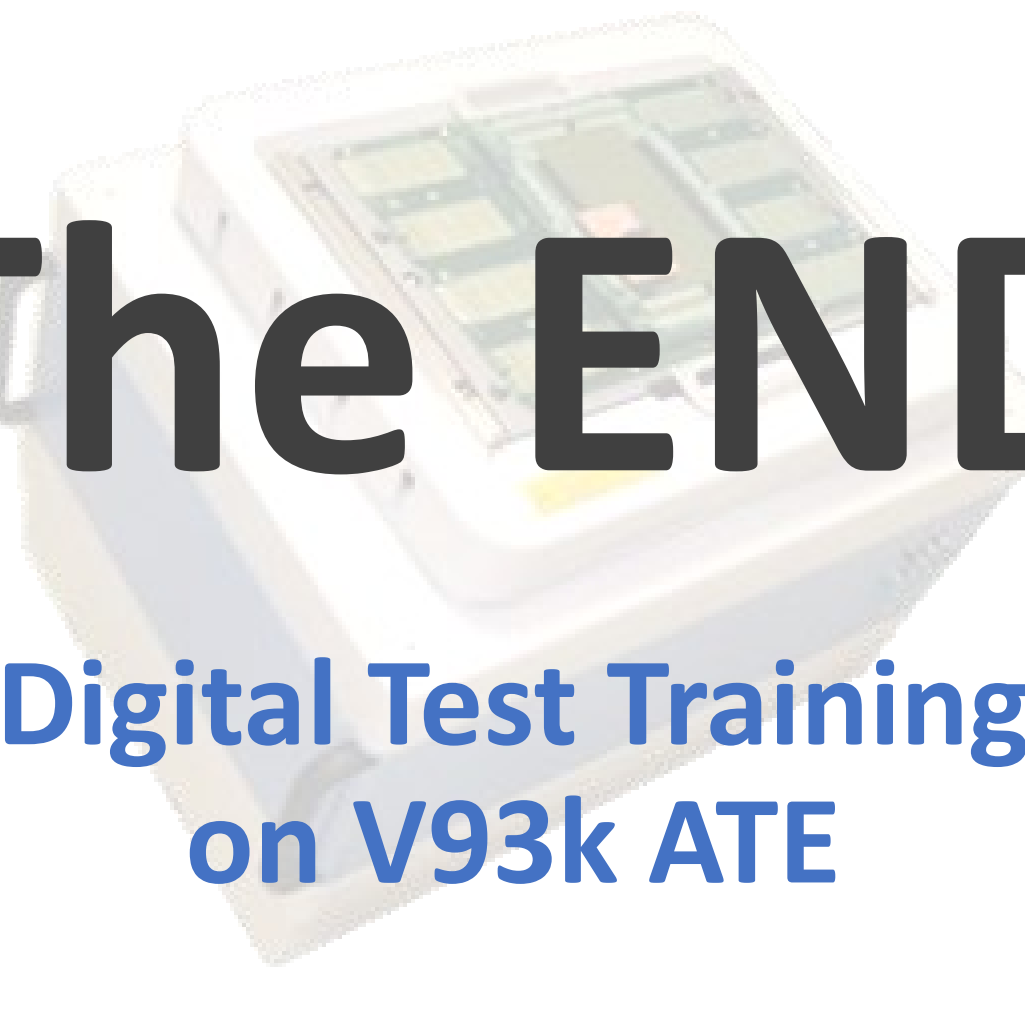
The screenshot shows the 'Test Control' window for the 'Prop Delay' test function. The window has a yellow background and a blue title bar. The 'Edit' and 'Doc' buttons are at the top left. The main area contains the following fields:

- Prop Delay** (circled in red)
- and Data Hold Time**
- pin list**: ser_out
- edge/param devcyc**: r1
- [ref. pin/time]**: LE
- [ref. devcyc]**: CP
- [pass prop delay]**: ns
- [pass data hold]**: ns
- Limit Value**: 15 (circled in red)
- output**: PD/DH (*P)

Arrows point from the 'Pin list' label to the 'ser_out' field and from the 'Edge under focus' and 'Reference (optional)' labels to the 'r1' and 'CP' fields respectively.

Lab & Exercises:

- Implementation of Parametric Tests
on 74ACT299 *(off-line + on-line)*
- Questions about Parametric Tests



The END

Digital Test Training
on V93k ATE